HD404918/HD404919/ HD40P4919

Description

The HD404918/HD404919/HD40P4919 CMOS 4-bit single-chip microcomputer of the HMCS400 series incorporates a ROM, RAM, I/O, and timer/counter, including high-voltage I/O pins and high-current output pins.

Features

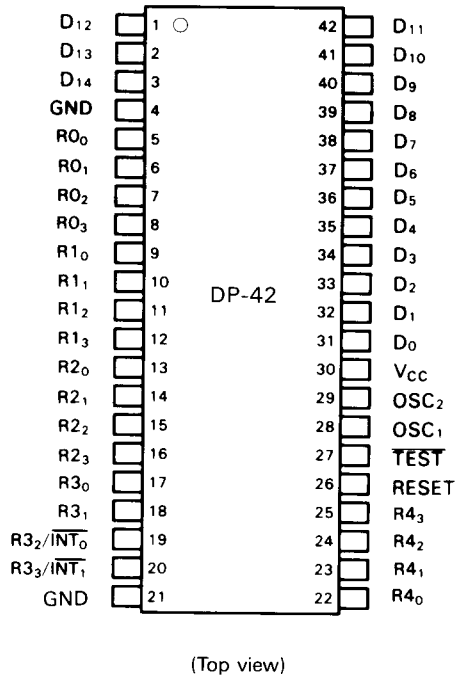
- 8192-word × 10-bit ROM (HD404918)
- 16384-word × 10-bit ROM (HD404919, HD40P4919)
  —HD40P4919 operates with an external EPROM (HN27C256 type)
- 512-digit × 4-bit RAM (HD404918)
- 992-digit × 4-bit RAM (HD404919, HD40P4919)
- 35 I/O pins, including 27 high-voltage I/O pins (12 V max.)
- Timer/counter
  —8-bit auto-reload timer/event counter
- Three interrupt sources
  —Two by external sources
  —One by timer/counter
- Subroutine stack up to 16 levels, including interrupts
- Minimum instruction execution time:
  —1.78μs (HD404918)
  —0.89μs (HD404919, HD40P4919)
- Low-power dissipation modes
  —Standby: Stops instruction execution while allowing clock oscillation and interrupt functions to operate
  —Stop: Stops instruction execution and clock oscillation while retaining RAM data
- On-chip oscillator
  —Crystal or ceramic filter (HD404918)
  An external clock is also available
  —Ceramic filter (HD404919, HD40P4919)
  An external clock is also available
- Standard 42-pin dual-inline plastic package (DP-42)
  42-pin dual-inline ceramic, EPROM on-package (DC-42P)

Ordering Information

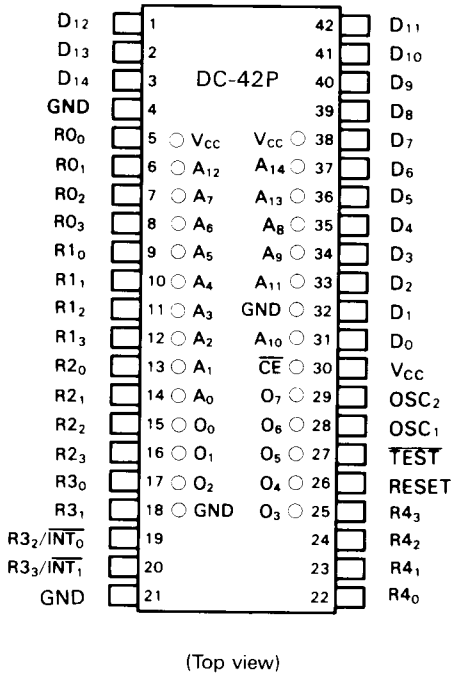
Type	Type Name	ROM (Words)	Mountable EPROM	f_{OSC} (MHz)*	Package
Mask ROM	HD404918	8,192	—	4	DP-42
	HD404919	16,384	—	8	DP-42
EPROM on-package	HD40P4919	16,384	HN27C256-20	4	DC-42P
			HN27C256H-85	8	

*Typical frequency

Pin Arrangement



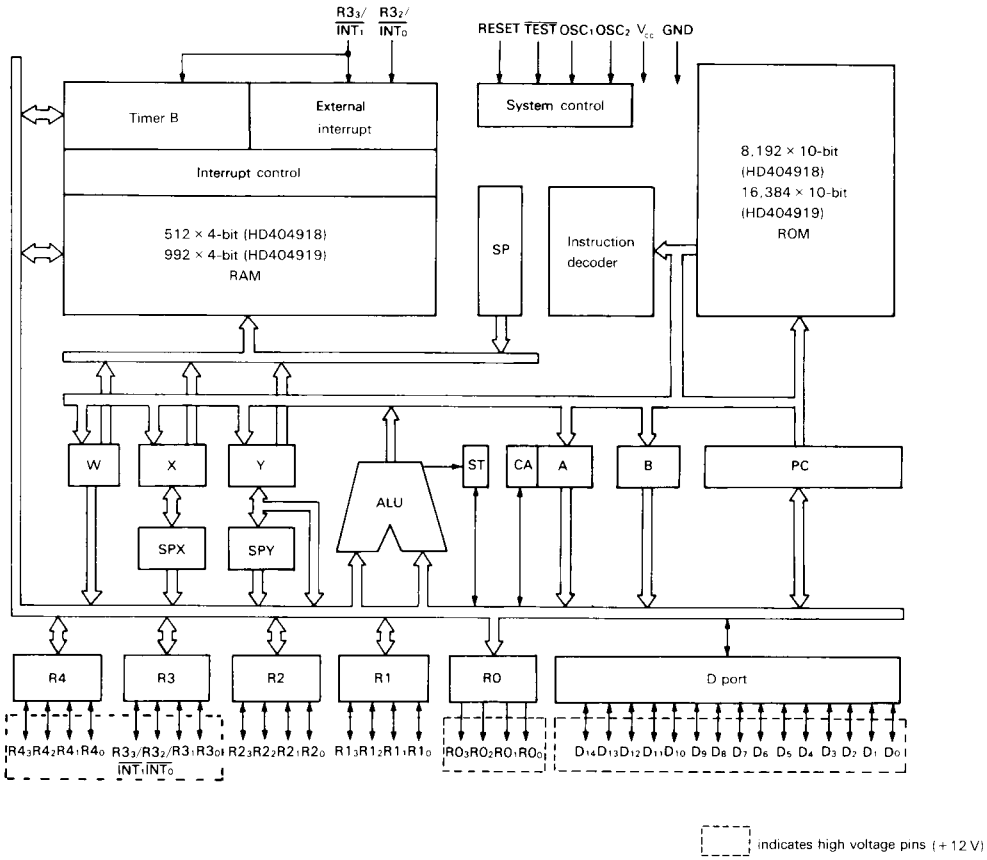
(Top view)



(Top view)

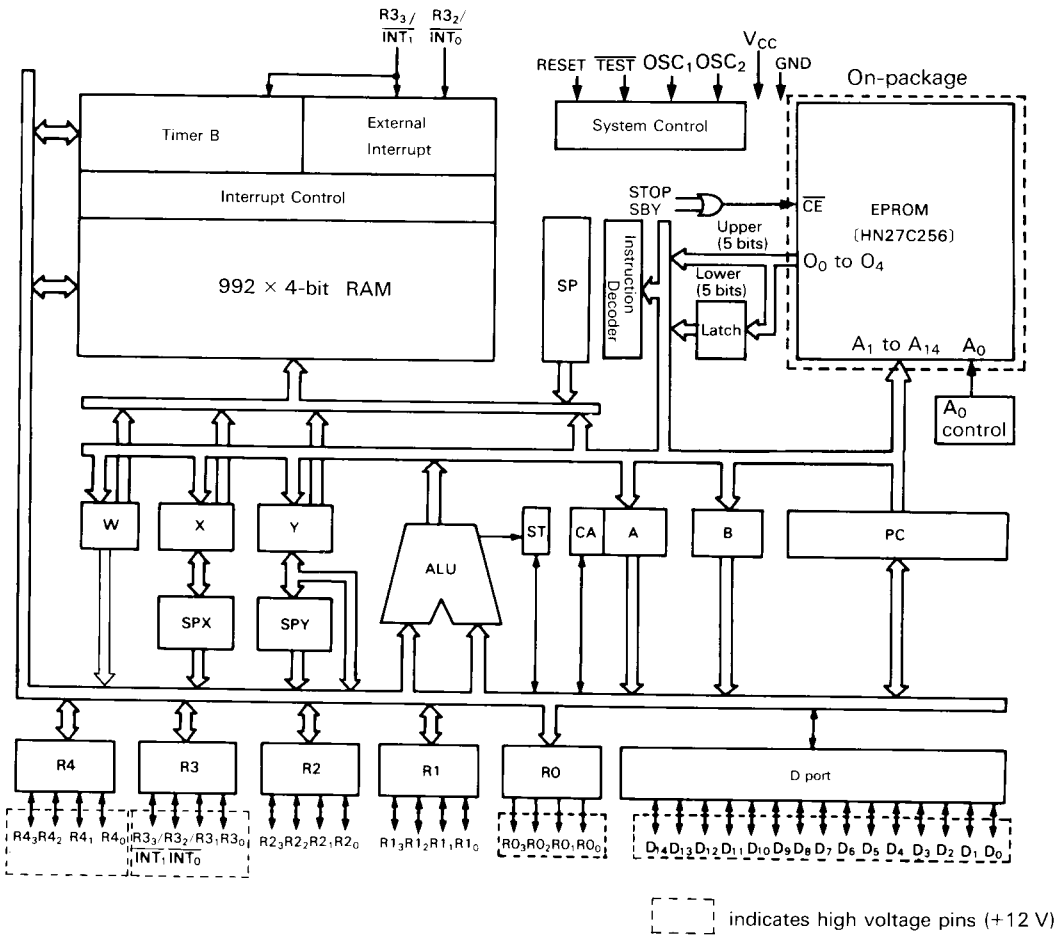
Block Diagram

HD404918/HD404919



Notes: 1. If without pull-up MOS is selected by the mask option, D_0-D_{14}, R0, R3, and R4 are used as high voltage pins.
2. If with pull-up MOS or CMOS is selected by the mask option, D_0-D_{14}, R0, R3, and R4 are used as standard pins.
3. If without pull-up MOS is selected for R1 and R2 they can be used as high current pins.

HD40P4919


R3₃/INT₁ R3₂/INT₀
Timer B
External Interrupt
Interrupt Control
992 × 4-bit RAM
RESET TEST OSC₁ OSC₂ Vcc GND
System Control
On-package
STOP SBY
Upper (5 bits)
Lower (5 bits)
Latch
SP
Instruction Decoder
CE
EPROM (HN27C256)
O₀ to O₄
A₁ to A₁₄ A₀
A₀ control
W
X
Y
SPX
SPY
ALU
ST
CA
A
B
PC
R4
R3
R2
R1
R0
D port
R4₃R4₂ R4₁ R4₀
R3₃/R3₂/R3₁R3₀ INT₁ INT₀
R2₃R2₂R2₁R2₀
R1₃R1₂R1₁R1₀
RO₃RO₂RO₁RO₀
D₁₄D₁₃D₁₂D₁₁D₁₀D₉D₈D₇D₆D₅D₄D₃D₂D₁D₀
indicates high voltage pins (+12 V)

Pin Functions

GND, V_{CC} (Power Supply)

Power supply pins for the MCU. Connect GND to ground (0 V) and apply the V_{CC} power supply voltage to the V_{CC} pin.

$\overline{TEST}$ (Test)

For test purposes only. Connect it to V_{CC}.

RESET (Reset)

MCU reset pin. For details, see the Reset section.

OSC_1, OSC_2 (Oscillator Connections)

Internal oscillator input pins. They can be connected to a ceramic filter resonator, crystal oscillator or external oscillator circuit. For details, see the Internal Oscillator Circuit section.

D_0-D_{14} (D Port)*

An input/output port addressed by the bit. These 15 pins are all input/output high-voltage pins. The circuit type for each pin can be selected using a mask option. For details, see the Input/Output section.

$R0_0-R0_3$, $R1_0-R1_3$, $R2_0-R2_3$, $R3_0-R3_3$, $R4_0-R4_3$ (R Ports)*

R0 to R4 are 4-bit ports. R0 is an output port, and R1 to R4 are I/O ports. R0, R3, and R4 are high-voltage ports, and R1 and R2 are high current ports. Each pin has a mask option which selects its circuit type. The pins $R3_2$ and $R3_3$ of port R3 are multiplexed with $\overline{INT_0}$ and $\overline{INT_1}$, respectively. For details, see the Input/Output section.

$\overline{INT_0}$, $\overline{INT_1}$ (Interrupts)

External interrupt pins. $\overline{INT_1}$ can be used as an external event input pin for timer B. $\overline{INT_0}$ and $\overline{INT_1}$ are multiplexed with $R3_2$ and $R3_3$, respectively. For details, see the Interrupt section.

* D_0-D_{14}, R0, R3, and R4 ports can be used as high voltage pins (12 V) only when without pull-up MOS option is selected.

Memory Map

ROM Memory Map

The MCU corresponding to its ROM capacity is shown in table 1. The ROM is described in the following paragraphs with the ROM memory map in figure 1.

Vector Address Area ($0000 to $000F): Locations $0000 through $000F are reserved for JMPL instructions to branch to the starting address of the initialization program and the interrupt programs. After a reset or an interrupt, the program is executed from the vector address.

Zero-Page Subroutine Area ($0000 to $003F): Locations $0000 through $003F are reserved for subroutines. The CAL instruction branches to these subroutines.

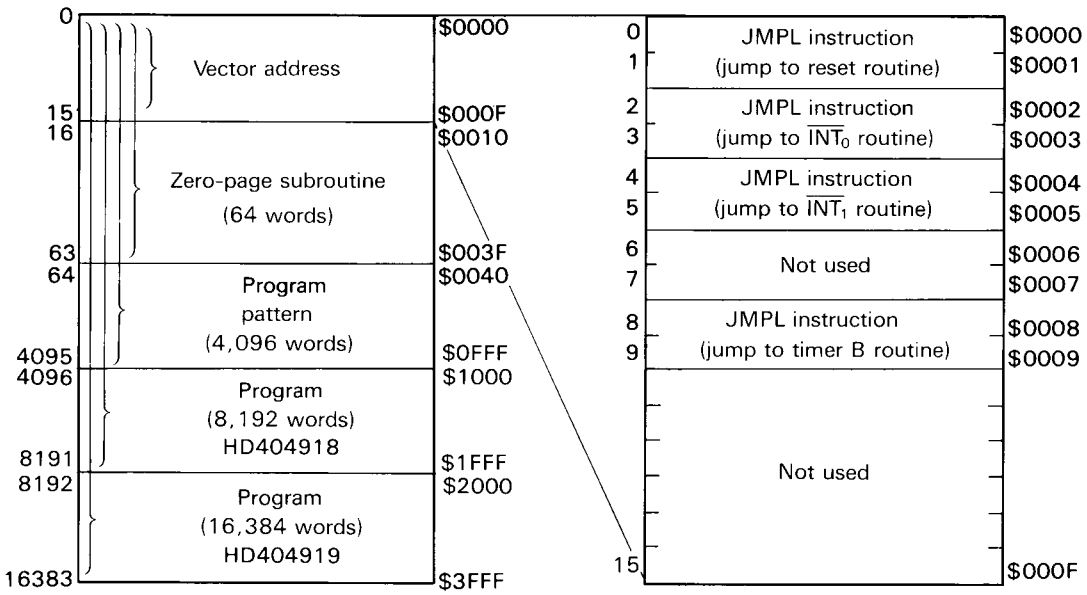
Pattern Area ($0000 to $0FFF): Locations $0000 through $0FFF are reserved for ROM data. The P instruction allows reference to the ROM data as a pattern.

Program Area ($0000 to $1FFF: HD404918; $0000 to $3FFF: HD404919, HD40P4919): Locations from $0000 through $1FFF and $0000 through $3FFF can be used for program code.

Table 1 ROM Capacity

Type Name	ROM Capacity
HD404918	8192 words × 10 bits
HD404919	16384 words × 10 bits
HD40P4919	

HD404918/HD404919 ROM Memory Map



HD40P4919 EPROM Memory Map

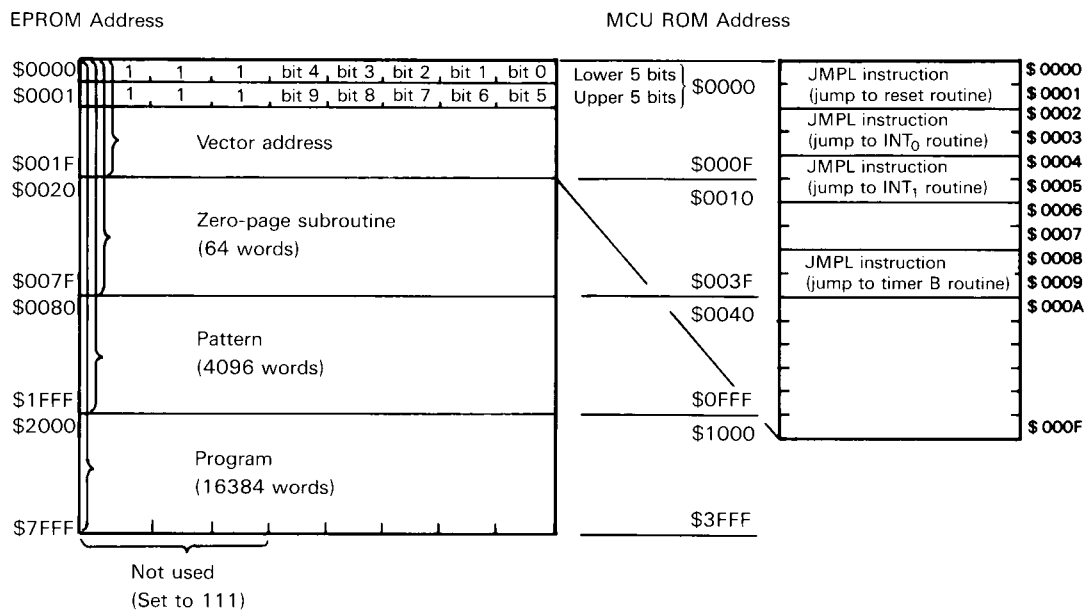


Figure 1 ROM Memory Maps

RAM Memory Map

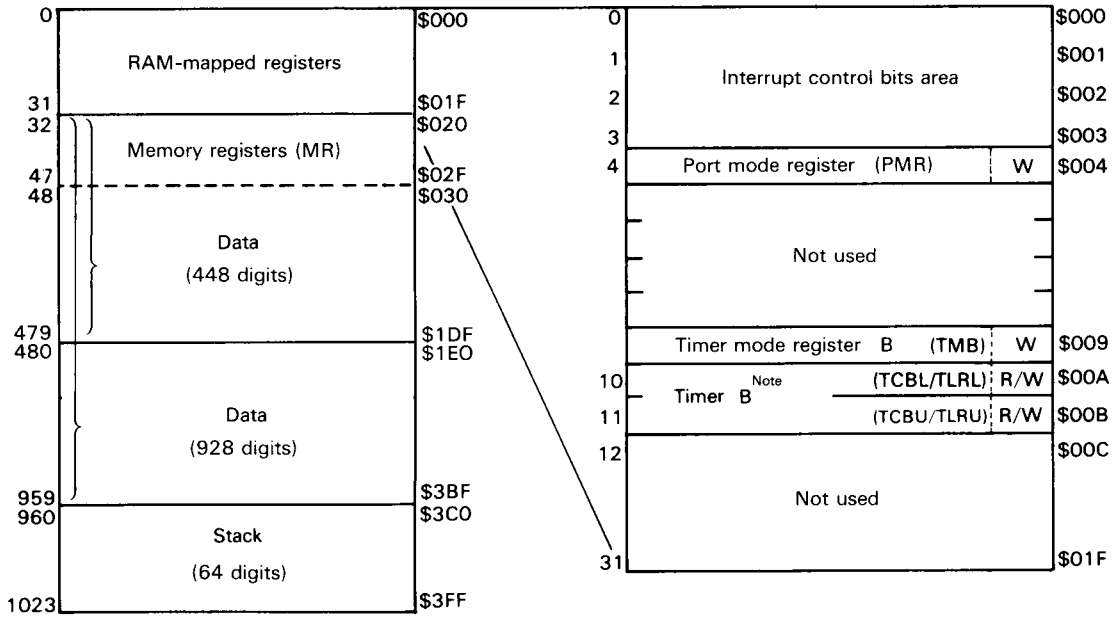
The corresponding MCU also contains RAM (table 2) as the data and stack area. In addition to these areas, interrupt control bits and special function registers are also mapped on the RAM memory space. The RAM memory map (figure 2) is described in the following paragraphs.

Interrupt Control Bits Area ($000 to $003): The interrupt control bits area (figure 3) is used for interrupt control. It is accessible only by RAM bit manipulation instructions. However, the interrupt request flag cannot be set by software. The RSP bit is used only to reset the stack pointer.

Special Function Registers Area ($004 to $00B): The special function registers are the mode or data registers for the external interrupts and the timer/counter. These registers are classified into three types: write-only, read-only, and read/write, as shown in figure 2. These registers cannot be accessed by RAM bit manipulation instructions.

Table 2 RAM Capacity

Type Name	RAM Capacity
HD404918	512 digits × 4 bits
HD404919	992 digits × 4 bits
HD40P4919	



Note: Two registers are mapped on the same address.

R: Read only
W: Write only
R/W: Read/Write

10	Timer counter B lower (TCBL)	R	Timer load register B lower (TLRL)	W	$00A
11	Timer counter B upper (TCBU)	R	Timer load register B upper (TLRU)	W	$00B

Figure 2 RAM Memory Map

Data Area ($020 to $1DF: HD404918; $020 to $3BF: HD404919, HD40P4919): The 16 digits, $020 through $02F, in the data area are called memory registers (MR) and are accessible by the LAMR and XMRA instructions (figure 4).

Stack Area ($3C0 to $3FF): Locations $3C0 through $3FF are reserved for LIFO stacks to save the contents of the program counter (PC), status flag (ST), and carry flag (CA) when subroutine calls (CAL or CALL instruction) and interrupts are processed. This area can be used as a 16-level nesting stack in which one level requires 4 digits. Figure 4 shows the save condition. The program counter is restored by the RTN and RTNI instructions. The status and carry flags are restored only by the RTNI instruction. This area, when not used as a stack, is available as a data area.

	Bit 3	Bit 2	Bit 1	Bit 0	
0	IM0 (IM of $\overline{INT_0}$)	IF0 (IF of $\overline{INT_0}$)	RSP (Reset SP bit)	IE (Interrupt enable flag)	$000
1	Not used	Not used	IM1 (IM of $\overline{INT_1}$)	IF1 (IF of $\overline{INT_1}$)	$001
2	Not used	Not used	IMTB (IM of timer B)	IFTB (IF of timer B)	$002
3	Not used	Not used	Not used	Not used	$003

IF: Interrupt request flag
IM: Interrupt mask
IE: Interrupt enable flag
SP: Stack pointer
Note: Each bit of the interrupt control bits area is set by the SEM/SEMD instruction, reset by the REM/REMD instruction, and tested by the TM/TMD instruction. It is not affected by other instructions. Furthermore, the interrupt request flag is not affected by the SEM/SEMD instruction. The value of the status flag becomes invalid when the unusable bits or the RSP bit is tested by the TM or TMD instruction.

Figure 3 Interrupt Control Bits Area Configuration

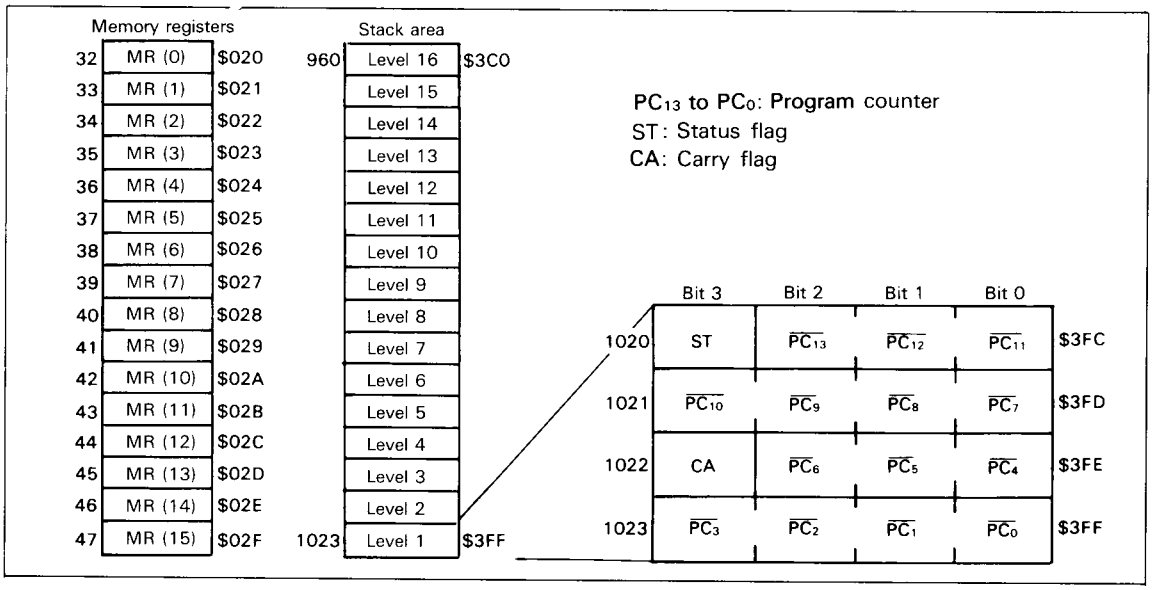


Figure 4 Configuration of Memory Registers, Stack Area, and Stack Position

Functional Description

Registers and Flags

The MCU has nine registers and two flags for CPU operations (figure 5).

Accumulator (A), B Register (B): The 4-bit accumulator and B register hold the results of the arithmetic logic unit (ALU), and transfer data to/from memory, I/O, and other registers.

W Register (W), X Register (X), Y Register (Y): The 2-bit W register and the 4-bit X and Y registers are used for indirect addressing of RAM. The Y register is also used for D-port addressing.

SPX Register (SPX), SPY Register (SPY): The 4-bit registers SPX and SPY assist the X and Y registers, respectively.

Carry Flag (CA): The carry flag (CA) stores the overflow from the ALU generated by an arithmetic operation. It is also affected by the SEC, REC, ROTL, and ROTR instructions.

During an interrupt, the carry flag is pushed onto the stack. It is restored by the RTNI instruction, but not by the RTN instruction.

Status Flag (ST): The status flag (ST) holds the ALU overflow, ALU non-zero, and the results of a bit test instruction for the arithmetic or compare instructions. It is a branch condition of the BR, BRL, CAL, or CALL instruction. The value of the status flag remains unchanged until the next arithmetic, compare, or bit test instruction is executed. The status flag becomes a 1 after the BR, BRL, CAL, or CALL instruction is executed or skipped. During an interrupt, the status flag is pushed onto the stack and restored back from the stack by the RTNI instruction, but not by the RTN instruction.

Program Counter (PC): The program counter is a 14-bit binary counter which controls the sequence in which the instructions stored in ROM are executed.

Stack Pointer (SP): The stack pointer (SP) is used to point to the address of the next stacking area (up to 16 levels).

The stack pointer is initialized to RAM address $3FF. It is decremented by 4 when data is pushed onto the stack, and incremented by 4 when data is restored from it. The stack can only be used up to 16 levels deep because the upper 4 bits of the stack pointer are fixed at 1111.

The stack pointer is initialized to $3FF either by MCU reset or by the RSP bit reset from the REM/REMD instruction.

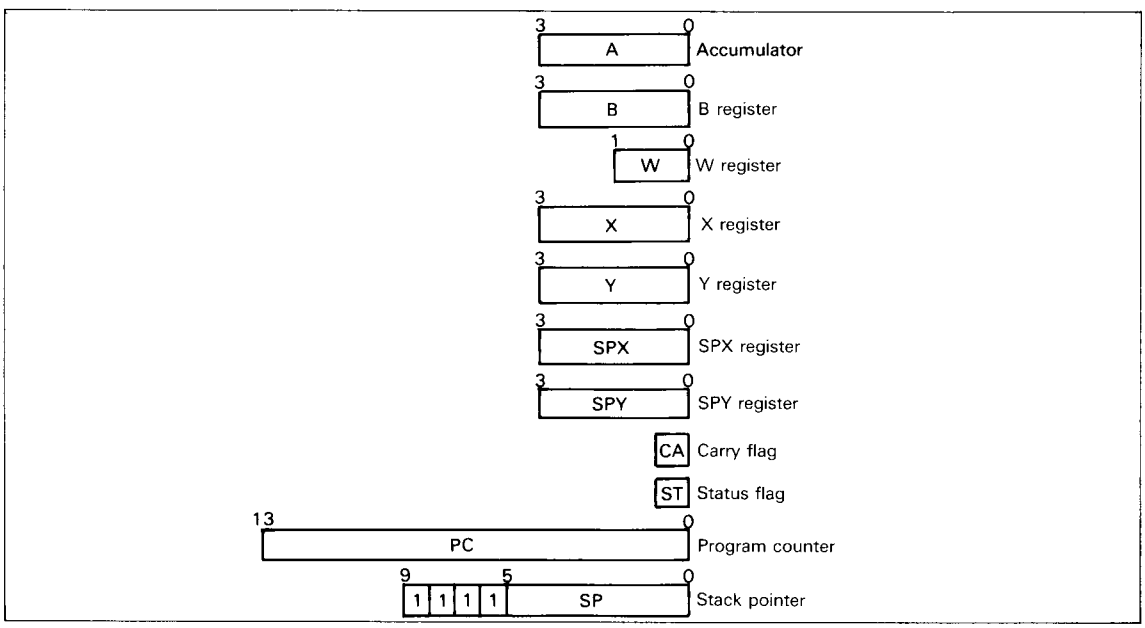


Figure 5 Registers and Flags

Interrupts

Three interrupt sources are available on the MCU: external requests ($\overline{INT_0}$, $\overline{INT_1}$) and a timer/counter (timer B). For each source, an interrupt request flag (IF), interrupt mask (IM), and interrupt vector addresses are provided to control and maintain the interrupt request. The interrupt enable flag (IE) is also used to control interrupt operations.

Interrupt Control Bits and Interrupt Servicing: The interrupt control bits are mapped on $000 through $003 of the RAM space. They are accessible by RAM bit manipulation instructions although the interrupt request flag (IF) cannot be set by software. The interrupt enable flag (IE) and IF are cleared to 0, and the interrupt mask (IM) is set to 1 after MCU reset.

Figure 6 is a block diagram of the interrupt control circuit. Table 3 shows the interrupt priority and vector addresses, and table 4 shows the interrupt conditions corresponding to each interrupt source.

Table 3 Vector Addresses and Interrupt Priority

Reset/Interrupt	Priority	Vector Addresses
RESET	—	$0000
$\overline{INT_0}$	1	$0002
$\overline{INT_1}$	2	$0004
Timer B	3	$0008

Table 4 Interrupt Conditions

Interrupt Control Bit	$\overline{INT_0}$	$\overline{INT_1}$	Timer B
IE	1	1	1
IF0·$\overline{IM0}$	1	0	0
IF1·$\overline{IM1}$	*	1	0
IFTB·$\overline{IMTB}$	*	*	1

* Don't care

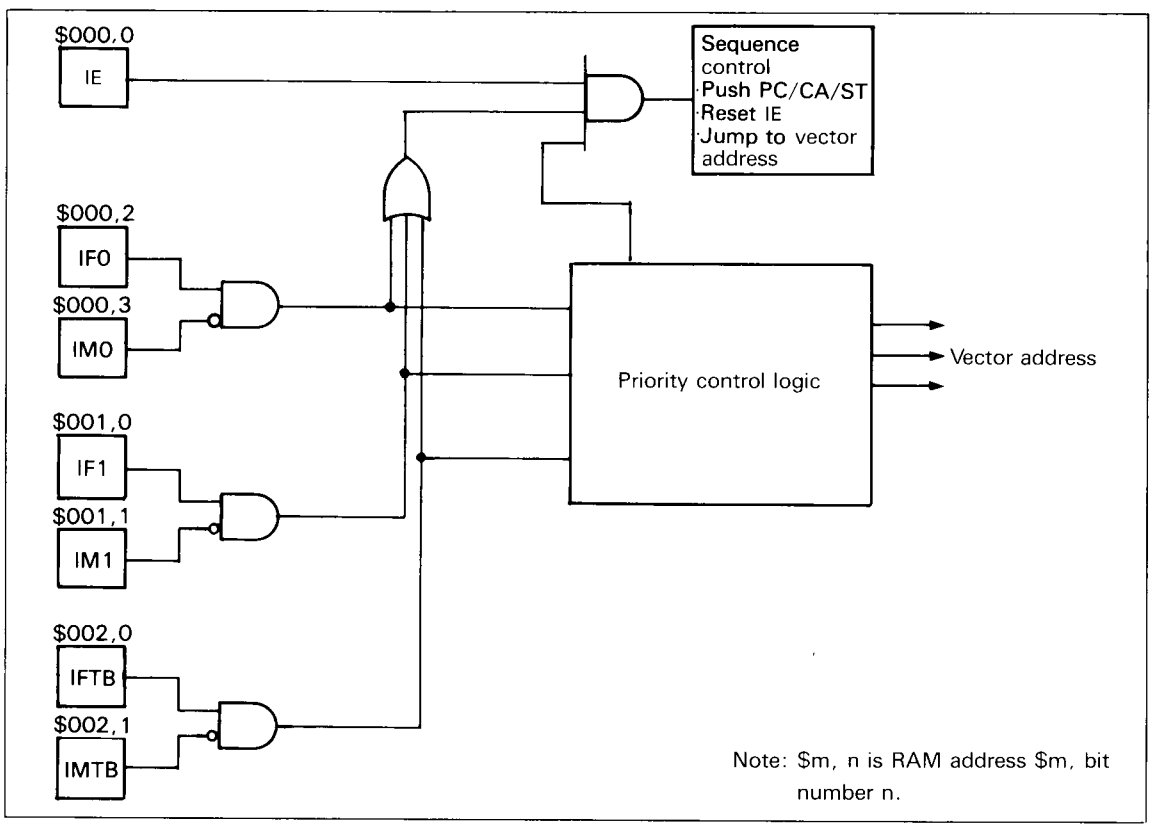


Figure 6 Interrupt Control Circuit Block Diagram

The interrupt request is generated when the IF is set to 1 and IM is 0. If the IE is 1 at this time, the interrupt will be activated and vector addresses will be generated from the priority PLA corresponding to the interrupt sources.

Figure 7 shows the interrupt processing sequence, and figure 8 shows the interrupt processing flowchart. If an interrupt is requested, the instruction being executed finishes in the first cycle, and the IE is reset in the second cycle. In the second and third cycles, the carry flag, status flag, and program counter are pushed onto the stack. Also in the third cycle, the instruction is re-executed after the MCU jumps to the vector address.

In each vector address, program the JMPL instruction to branch to the starting address of the interrupt program. The IF which caused the interrupt must be reset by software in the interrupt program.

Interrupt Enable Flag (IE: $000, Bit 0): The interrupt enable flag enables/disables interrupt requests as shown in table 5. It is reset by an interrupt and set by the RTNI instruction.

External Interrupts ($\overline{INT_0}$, $\overline{INT_1}$): The external interrupt request inputs ($\overline{INT_0}$, $\overline{INT_1}$) can be selected by the port mode register (PMR: $004). Setting bit 3 and bit 2 of PMR causes the $R3_3/\overline{INT_1}$ and $R3_2/\overline{INT_0}$ pins to be used as $\overline{INT_1}$ and $\overline{INT_0}$, respectively.

The external interrupt request flags (IF0, IF1) are set at the falling edge of $\overline{INT_0}$ and $\overline{INT_1}$ inputs. (Refer to table 6.)

The $\overline{INT_1}$ input can be used as a clock signal input to timer B, in which timer B counts up at each falling edge of the $\overline{INT_1}$ input. When $\overline{INT_1}$ is used as the timer B external event input, the external interrupt mask (IM1) has to be set so that the interrupt request by $\overline{INT_1}$ will not be accepted. (Refer to table 7.)

External Interrupt Request Flags (IF0: $000, Bit 2; IF1: $001, Bit 0): The external interrupt request flags (IF0, IF1) are set at the falling edge of the $\overline{INT_0}$ and $\overline{INT_1}$ inputs, respectively.

External Interrupt Masks (IM0: $000, Bit 3; IM1: $001, Bit 1): The external interrupt masks mask the external interrupt requests.

Port Mode Register (PMR: $004): The port mode register is a 4-bit write-only register which controls the $R3_2/\overline{INT_0}$ and $R3_3/\overline{INT_1}$ pins as shown in table 8. The port mode register will be initialized to $0 by MCU reset. These pins are therefore initially used as ports.

Table 5 Interrupt Enable Flag

IE	Interrupt Enable/Disable
0	Disable
1	Enable

Table 6 External Interrupt Request Flags

IF0, IF1	Interrupt Requests
0	No
1	Yes

Table 7 External Interrupt Masks

IM0, IM1	Interrupt Requests
0	Enable
1	Disable (Mask)

Table 8 Port Mode Register

PMR3	$R3_3/\overline{INT_1}$ Pin
0	Used as $R3_3$ port input/output pin
1	Used as $\overline{INT_1}$ input pin

PMR2	$R3_2/\overline{INT_0}$ Pin
0	Used as $R3_2$ port input/output pin
1	Used as $\overline{INT_0}$ input pin

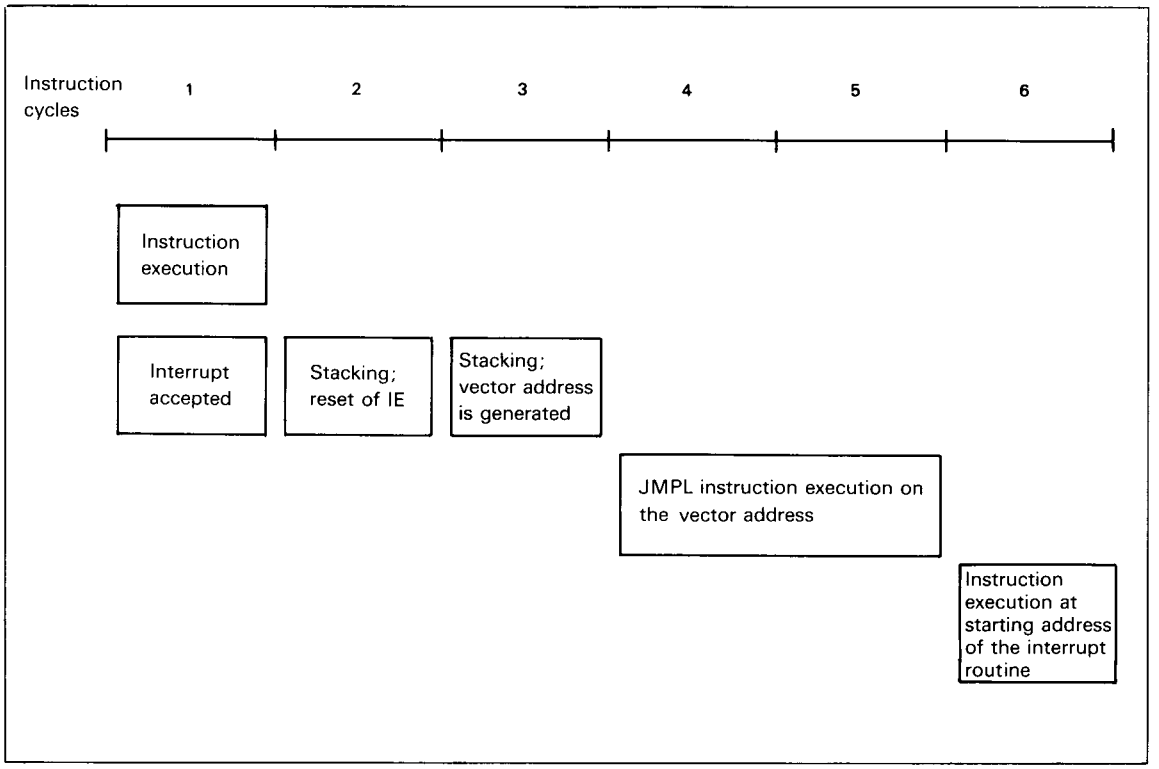


Figure 7 Interrupt Processing Sequence

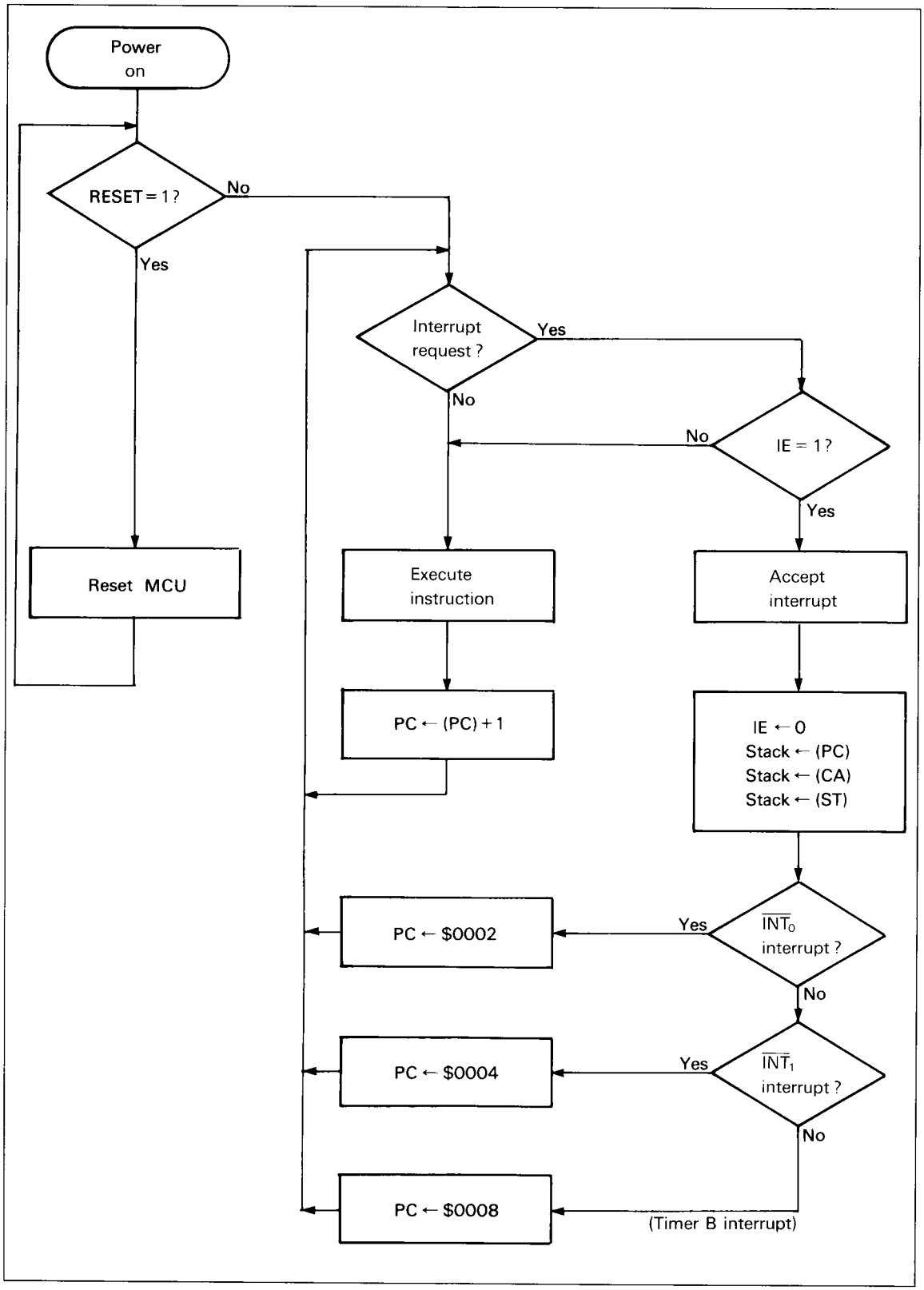


Figure 8 Interrupt Processing Flowchart

Timer

The MCU contains a prescaler and a timer/counter (timer B shown in figure 9) whose functions are the same as the HMCS404C. The prescaler is an 11-bit binary counter, and timer B is an 8-bit auto-reload timer/event counter.

Prescaler: The input to the prescaler is a system clock signal. The prescaler is initialized to $000 by MCU reset, and starts to count up the system clock signal as soon as reset input goes to logic 0. The prescaler keeps counting up except at MCU reset and stop mode. The prescaler provides clock signals to timer B. The prescaler divide ratio is selected by timer mode register B (TMB).

Timer B Operation: Timer mode register B (TMB: $009) selects the auto-reload function, input clock source, and the prescaler divide ratio for timer B. When the external event input is used as an input clock signal to timer B, select $R3_3/\overline{INT_1}$ as $\overline{INT_1}$ and set the external interrupt mask (IM1) to prevent an external interrupt request from occurring.

Timer B is initialized according to the data written into timer load register B by software. Timer B counts up at every clock input signal. When the next clock signal is applied to timer B after it is set to $FF, it will generate an overflow output. In this case, if the autoreload function is selected, timer B is initialized according to the value of timer load register B. If it is not selected, timer B goes to $00. The timer B interrupt request flag (IFTB: $002, bit 0) will be set as this overflow output.

Timer Mode Register B (TMB: $009): Timer mode register B (TMB) is a 4-bit write-only register which selects the auto-reload function, the prescaler divide ratio, and the source of the clock input signal, as shown in table 9. Timer mode register B is initialized to $0 by MCU reset.

The operation mode of timer B changes at the second instruction cycle after timer mode register B is written to. Initialization of timer B by writing data into timer load register B should be performed after the contents of TMB are changed. Configuration and function of timer mode register B is shown in figure 10.

Timer B (TCBL: $00A, TCBU: $00B, TLRL: $00A, TLRU: $00B): Timer B consists of an 8-bit write-only timer load register and an 8-bit read-only timer counter. Each of them has a low-order digit (TCBL: $00A, TLRL: $00A) and a high-order digit (TCBU: $00B, TLRU: $00B). (Refer to figure 2.)

Timer counter B can be initialized by writing data into timer load register B. In this case, write the low-order digit first, and then the high-order digit. The timer counter is initialized when the high-order digit is written. The timer load register is initialized to $00 by MCU reset.

The counter value of timer B can be obtained by reading timer counter B. In this case, read the high-order digit first, and then the low-order digit. The count value of the low-order digit is latched when the high-order digit is read.

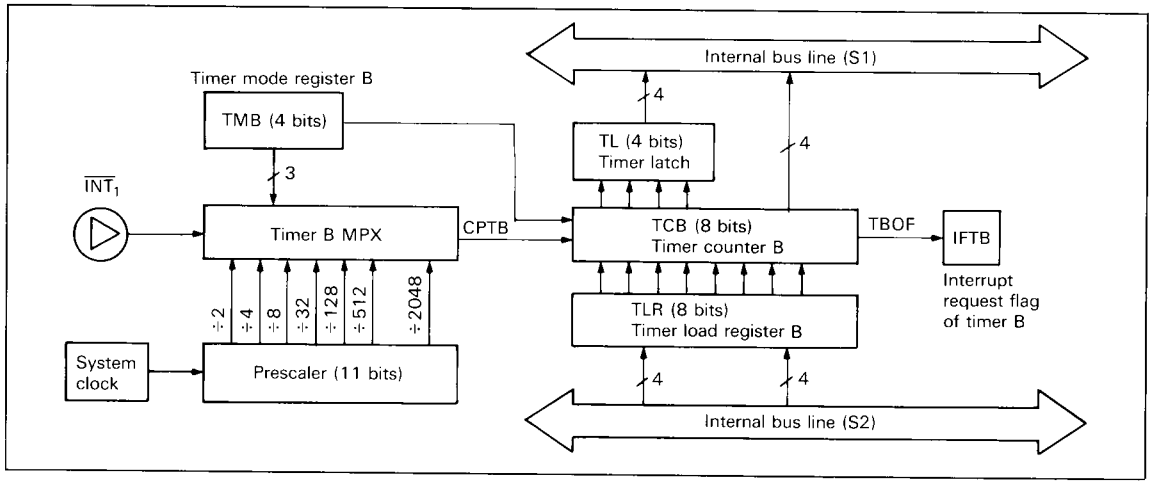


Figure 9 Timer/Counter Block Diagram

Timer B Interrupt Request Flag (IFTB: $002, Bit 0): The timer B interrupt request flag is set by the overflow output of timer B (table 10).

Timer B Interrupt Mask (IMTB: $002, Bit 1): The timer B interrupt mask prevents an interrupt request from being generated by the timer B interrupt request flag (table 11).

Table 9 Timer Mode Register B

TMB3	Auto-Reload Function
0	No
1	Yes

TMB2	TMB1	TMB0	Prescaler Divide Ratio, Clock Input Source
0	0	0	÷2048
0	0	1	÷512
0	1	0	÷128
0	1	1	÷32
1	0	0	÷8
1	0	1	÷4
1	1	0	÷2
1	1	1	$\overline{INT_1}$ (External event input)

Table 10 Timer B Interrupt Request Flag

IFTB	Interrupt Request
0	No
1	Yes

Table 11 Timer B Interrupt Mask

IMTB	Interrupt Request
0	Enable
1	Disable (Mask)

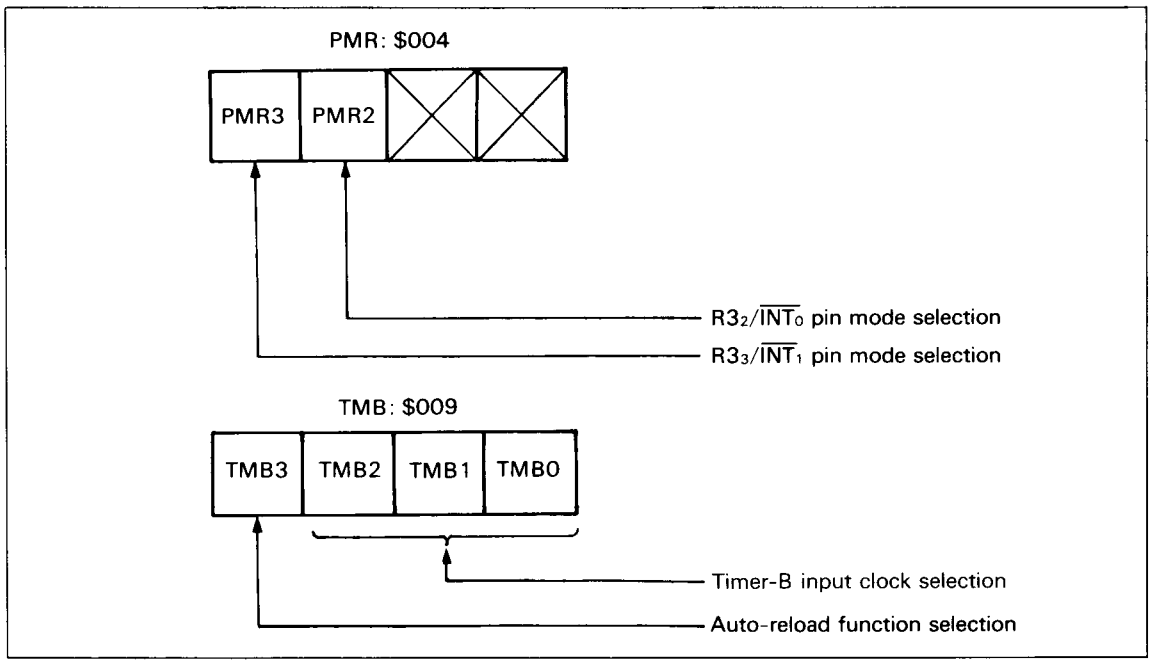


Figure 10 Mode Register Configuration and Function

Input/Output

The MCU has 35 I/O pins, 8 standard and 27 high voltage. One of three circuit types can be selected by the mask option for each high-voltage pin: (A) without pull-up MOS (NMOS open drain), (B) with pull-up MOS, or (C) CMOS. High-voltage pins can be used as high-voltage I/O pins only when (A) is selected, except for R1 and R2. R1 and R2 are fixed as mask option A.

When any input/output pin is used as an input pin, the mask option and output data must be selected in the manner specified in table 13.

Output Circuit Operation of With Pull-Up MOS Standard Pins: By the standard pin option with pull-up MOS, the circuit shown in figure 11 shortens the rise time of the output.

When the MCU executes an output instruction, it generates a write pulse to the R port addressed by this instruction. This pulse will switch the PMOS (B) on and shorten the rise time. The write pulse keeps PMOS in the on state for one-eighth of the instruction cycle time. While the write pulse is 0, a high output level is maintained by the pull-up MOS (C).

When the $\overline{HLT}$ signal becomes 0 in stop mode, MOSs (A), (B), and (C) turn off.

D Port: The D port has 15 discrete I/O pins, each of which can be addressed independently. It can be set/reset through the SED/RED and SEDD/REDD instructions, and can be tested through the TD and TDD instructions. See table 12 for the I/O pin circuit types.

R Ports: The five R ports are composed of 16 I/O pins and 4 output-only pins. Data is input through the LAR and LBR instructions and output through the LRA and LRB instructions. The MCU is not affected when the input-only and/or non-existing ports are written into, however invalid data will be read from the output-only and/or non-existing ports.

The $R3_2$ and $R3_3$ pins are multiplexed with the $\overline{INT_0}$ and $\overline{INT_1}$ pins, respectively. See table 12 for the selectable circuit types for these I/O pins.

Unused I/O Pins: If unused I/O pins are left floating, the LSI may malfunction due to noise. The I/O pins should be fixed as follows to prevent malfunction.

High-voltage pins: Unused pins should be pulled up to V_{CC} on the printed circuit board.

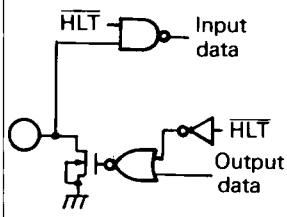
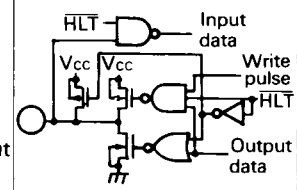
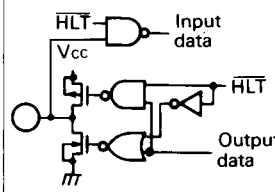
Standard pins: Unused pins should be pulledup to V_{CC} on the printed circuit board.

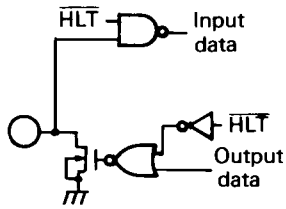
Reset

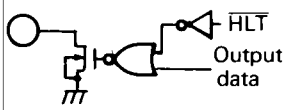
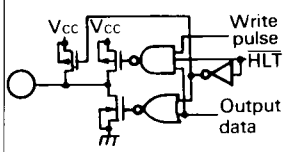
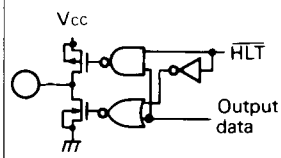
Setting the RESET pin high resets the MCU. At power-on or when stop mode is cancelled, the reset must satisfy the time t_{RC} for the oscillator to stabilize. In all other cases, at least two instruction cycles are required for the MCU to be reset.

Table 14 shows the components initialized by MCU reset, and the status of each.

Table 12 I/O Pin Circuit Types

	Without Pull-Up MOS (NMOS Open Drain) (A)	With Pull-Up MOS (B)	CMOS (C)	Pins
I/O Pins				D_0-D_{14} $R3_0$-$R3_3$ $R4_0$-$R4_3$
High current	Not available	Not available	Not available	
High voltage	Available	Not available	Not available	

	Without Pull-Up MOS (NMOS Open Drain) (A)	pins
I/O Pins		$R1_0$-$R1_3$ $R2_0$-$R2_3$
High current	Available	
High voltage	Not available	

	Without Pull-Up MOS (NMOS Open Drain) (A)	With Pull-Up MOS (B)	CMOS (C)	Pins
Output Pins				RO_0-RO_3
High current	Not available	Not available	Not available	
High voltage	Available	Not available	Not available	

Notes: 1. If without pull-up MOS is selected by the mask option, D_0-D_{14}, R0, R3, and R4 are used as high-voltage pins.
2. If with pull-up MOS or CMOS is selected by the mask option, D_0-D_{14}, R0, R3, and R4 are used as standard pins.
3. Ports R1 and R2 are high-current pins having only without pull-up MOS.

Table 13 Data Input from Common Input/Output Pins

I/O Pin Circuit Type	Input Possible	Input Pin State
CMOS	No	—
Without pull-up MOS (NMOS open drain)	Yes	1
With pull-up MOS	Yes	1

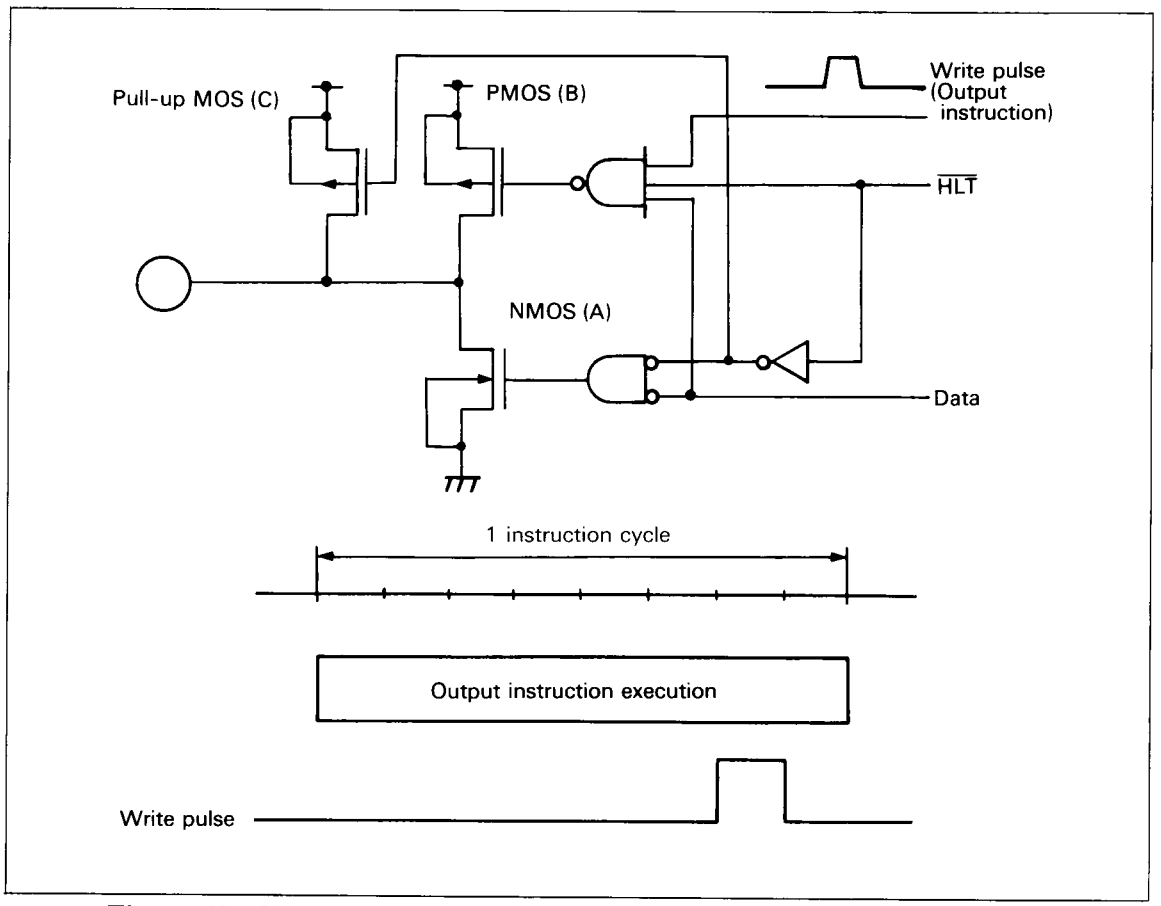


Figure 11 Output Circuit Operation of Pins With Pull-Up MOS Option

Note: The mask option of the circuit type is shown in the table below. The mask ROM type MCU is compatible with the EPROM on-package type MCU only when the mask ROM type MCU is selected as type A.

	Circuit type		
Product type	**A**	**B**	**C**
Mask ROM Type (HD404918, HD404919)	Optional	Optional	Optional
EPROM On-Package Type (HD40P4919)	fixed	–	–

Table 14 Initial Values After MCU Reset

Item		Initial Value by MCU Reset	Contents
Program counter (PC)		$0000	Execute the program from the top of ROM address
Status flag (ST)		1	Enable branching with conditional branch instructions
Stack pointer (SP)		$3FF	Stack level is 0
I/O pins, output registers	(A) Without pull-up MOS	1	Enable input
	(B) With pull-up MOS	1	Enable input
	(C) CMOS	1	—
Interrupt flags/ mask	Interrupt enable flag (IE)	0	Inhibit all interrupts
	Interrupt request flag (IF)	0	No interrupt request
	Interrupt mask (IM)	1	Mask interrupt request
Mode registers	Port mode register (PMR)	0000	See Port Mode Register section
	Timer mode register B (TMB)	0000	See Timer Mode Register B section
Timer/counter	Prescaler	$000	—
	Timer counter B (TCB)	$00	—
	Timer load register B (TLR)	$00	—

Note: MCU reset affects the other registers as shown in the following table.

Item		After MCU Reset to Recover from Stop Mode	After MCU Reset to Recover from Other Modes
Carry flag	(CA)	The contents of the items before MCU reset are not guaranteed, therefore they must be initialized by software.	The contents of the items before MCU reset are not guaranteed, therefore they must be initialized by software.
Accumulator	(A)		
B register	(B)		
W register	(W)		
X/SPX registers	(X/SPX)		
Y/SPY registers	(Y/SPY)		
RAM		The contents of RAM before MCU reset (just before STOP instruction) are retained.	Same as above for RAM.

Internal Oscillator Circuit

Figure 12 is a block diagram of the internal oscillator circuit. In addition, figure 13 shows the layout of the crystal or ceramic filter. An external clock operation is also available.

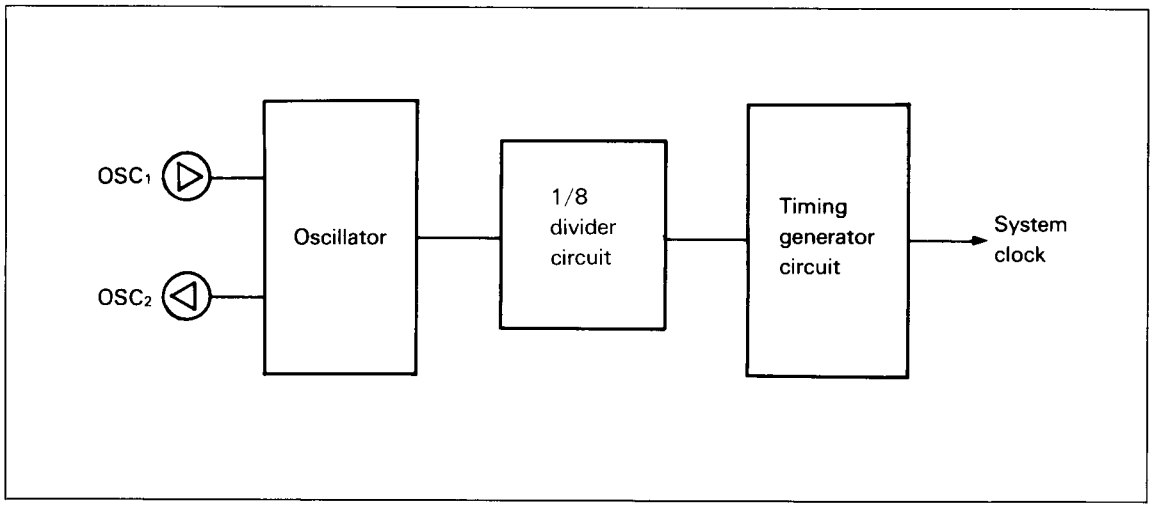


Figure 12 Internal Oscillator Circuit

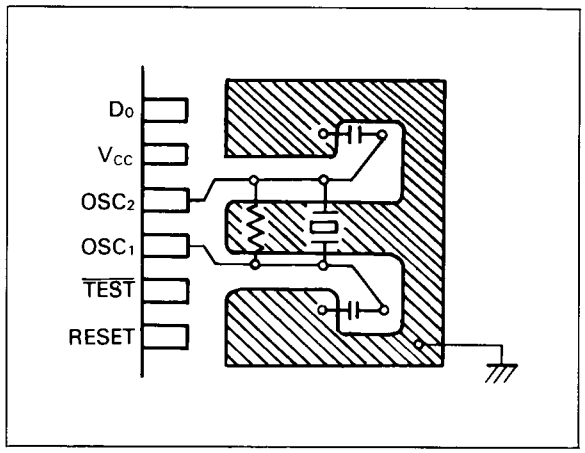
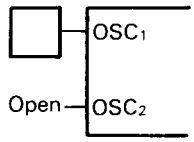
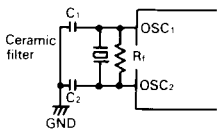
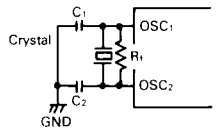
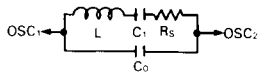


Figure 13 Layout of Crystal and Ceramic Filter

Table 15 Examples of Oscillator Circuits

	Circuit Configuration	Circuit Constants	
		HD404918	HD404919/HD40P4919
External clock operation	Oscillator 		
Ceramic filter oscillator		Ceramic filter CSA 4.00MG (Murata) R_f: 1 MΩ ± 20% C_1: 30 pF ± 20% C_2: 30 pF ± 20%	Ceramic filter CSA 8.00MT (Murata) R_f: 1 MΩ ± 20% C_1: 30 pF ± 20% C_2: 30 pF ± 20%
Crystal oscillator	 AT-cut parallel resonance crystal 	R_f: 1 MΩ ± 20% C_1: 10-22 pF ± 20% C_2: 10-22 pF ± 20% Crystal: Equivalent circuit shown at bottom left C_0: 7 pF max. R_S: 100 Ω max. f: 1.0–4.5 MHz	

Notes: 1. The circuit parameters written above are recommended by the crystal or ceramic filter maker. The circuit parameters are affected by the crystal, ceramic filter resonator, and the floating capacitance when designing the board. When designing the oscillator circuit, consult with the crystal or ceramic filter maker to determine the circuit parameters.

2. Wiring among OSC_1, OSC_2, and other elements should be as short as possible, and avoid crossing other wires. Refer to the recommended layout of the crystal and ceramic filter in figure 13.

Low-Power Dissipation Modes

The MCU has two low-power dissipation modes, standby mode and stop mode (table 16). Figure 14 is a mode transition diagram for these modes.

Standby Mode: Executing the SBY instruction places the MCU into standby mode. In standby mode, the oscillator circuit is active, and interrupts and the timer/counter remain working. On the other hand, the CPU stops since the clock related to the instruction execution stops. Registers, RAM, and I/O pins retain the states they were in just before the MCU went into standby mode.

Table 16 Low-Power Dissipation Modes

Condition	Standby Mode	Stop Mode
Instruction	SBY instruction	STOP instruction
Oscillator circuit	Active	Stopped
Instruction execution	Stopped	Stopped
Registers, flags	Retained	Reset (Note 1)
Interrupt function	Active	Stopped
RAM	Retained	Retained
Input/output pins	Retained (Note 2)	High impedance
Timer/counter	Active	Stopped
Cancellation method	RESET input, interrupt request	RESET input

Notes: 1. The MCU recovers from stop mode by RESET input. Refer to table 14 for the contents of flags and registers.
2. When I/O circuits are active, an I/O current may flow in standby mode, depending on the state of the I/O pins. This is an additional current added to the standby mode current dissipation.

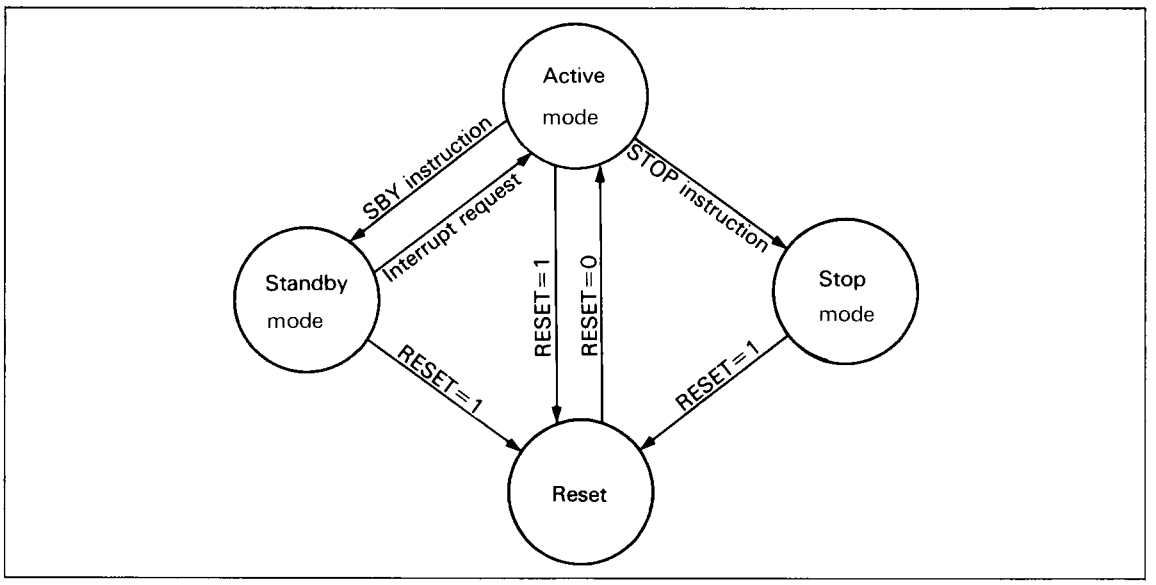


Figure 14 MCU Operation Mode Transition

The standby mode may be cancelled by inputting RESET or by asserting an interrupt request. In the former case the MCU is reset. If the interrupt enable flag is 1 at this time, the interrupt is executed; if it is 0, the interrupt request is put on hold and normal instruction execution continues. In the latter case, the MCU becomes active and executes the next instruction following the SBY instruction.

Figure 15 shows the flowchart of the standby mode.

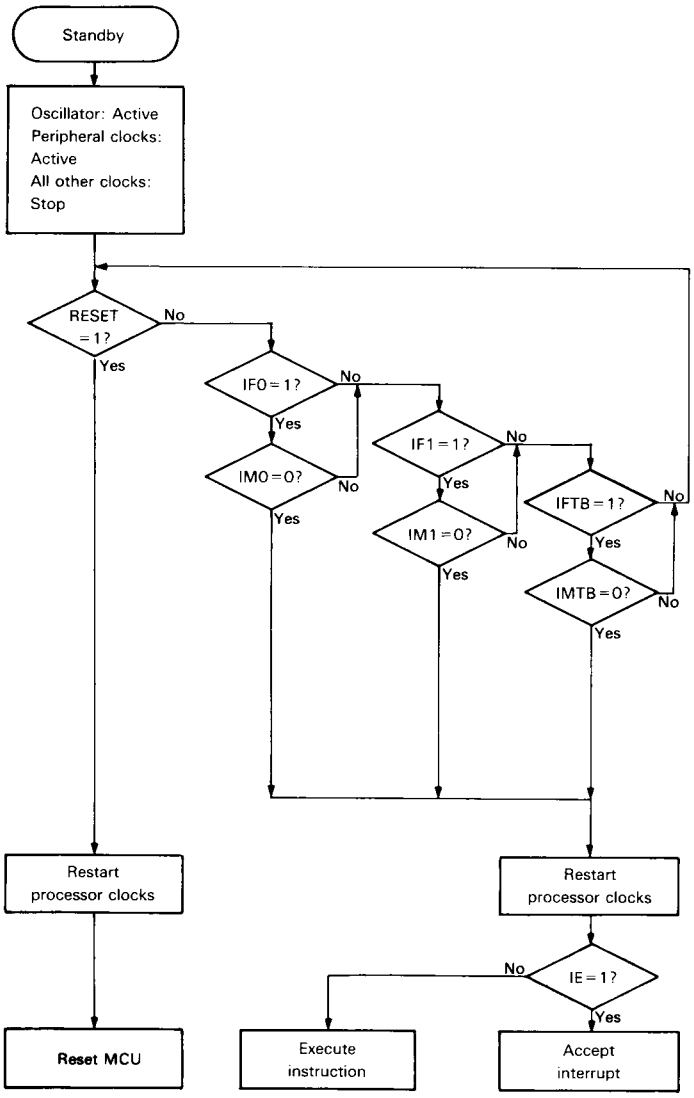


Figure 15 MCU Standby Mode Operation Flowchart

Stop Mode: Executing the STOP instruction brings the MCU into stop mode, in which the oscillator circuit and every function of the MCU stop.

The stop mode may be cancelled by resetting the MCU. At this time, as shown in figure 16, the reset input must be applied for at least t_{RC} in order for oscillation to stabilize. (Refer to the AC Characteristics table.) After stop mode is cancelled, the RAM retains the state it was in just before the MCU went into stop mode, but the accumulator, B register, W register, Y/SPY registers, and carry flag will not retain their contents.

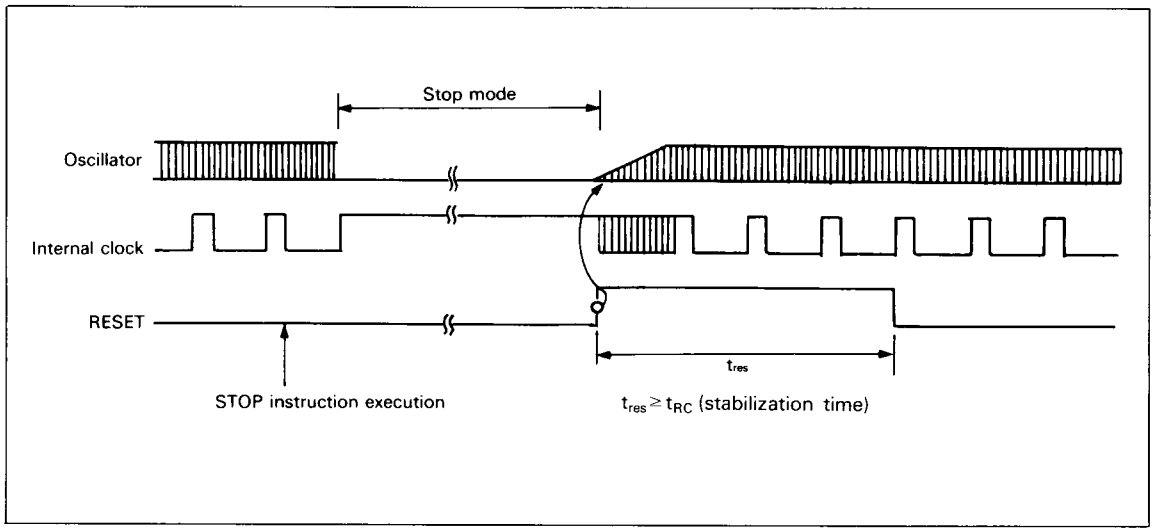


Figure 16 Timing of Stop Mode Cancellation

Addressing Modes

RAM Addressing Modes

As shown in figure 17, the MCU has three RAM addressing modes: register indirect addressing, direct addressing, and memory register addressing.

Register Indirect Addressing Mode: The W register, X register, and Y register contents (10 bits total) are used as the RAM address.

Direct Addressing Mode: A direct addressing instruction consists of two words, with the word (10 bits) following the opcode used as the RAM address.

Memory Register Addressing Mode: The memory registers (16 digits from $020 to $02F) are accessed by executing the LAMR and XMRA instructions.

ROM Addressing Modes and the P Instruction

The MCU has four ROM addressing modes as shown in figure 18.

Direct Addressing Mode: The program can branch to any address in ROM memory space by executing the JMPL, BRL, or CALL instruction. These instructions replace the 14 program counter bits (PC_{13} to PC_0) with 14-bit immediate data.

Current Page Addressing Mode: The MCU has 32 pages of ROM with 256 words per page. By executing the BR instruction, the program can branch to an address on the current page. This instruction replaces the low-order eight bits of the program counter (PC_7 to PC_0) with 8-bit immediate data.

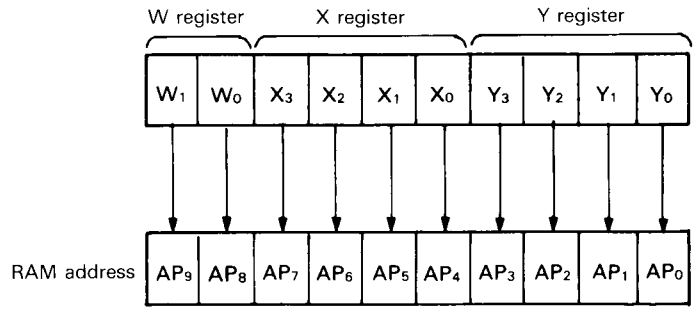
When the BR instruction is on a page boundary (256n + 255) (figure 19), executing it transfers the PC contents to the next page because of the hardware architecture. Consequently, the program branches to the next page when the BR instruction is used on a page boundary. The HMCS400 series cross macroassembler has an automatic paging facility for ROM pages.

Zero-Page Addressing Mode: By executing the CAL instruction, the program can branch to the zero-page subroutine area, which is located at $0000-$003F. When the CAL instruction is executed, 6-bits of immediate data are placed in the low-order six bits of the program counter (PC_5 to PC_0) and 0s are placed in the high-order eight bits (PC_{13} to PC_6).

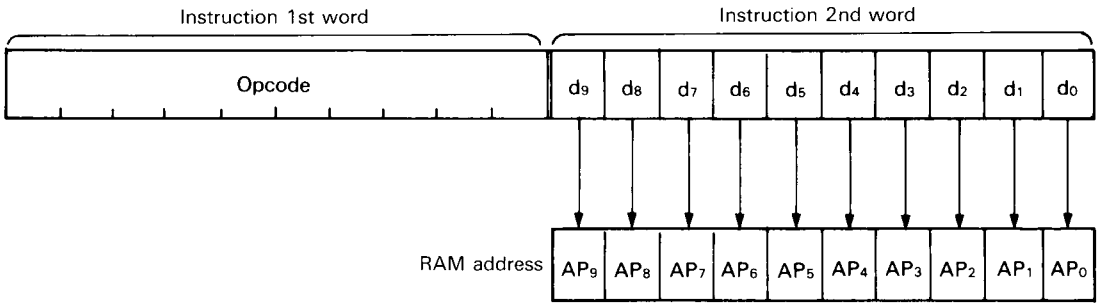
Table Data Addressing Mode: By executing the TBR instruction, the program can branch to the address determined by the contents of the 4-bit immediate data, accumulator, and B register.

P Instruction: ROM data addressed by table data addressing can be referenced by the P instruction (figure 20). When bit 8 of the referred ROM data is 1, 8 bits of ROM data are written into the accumulator and B register. When bit 9 is 1, 8 bits of ROM data are written into the R1 and R2 port output registers. When both bits 8 and 9 are 1, ROM data are written into the accumulator and B register, and also to the R1 and R2 port output registers at the same time.

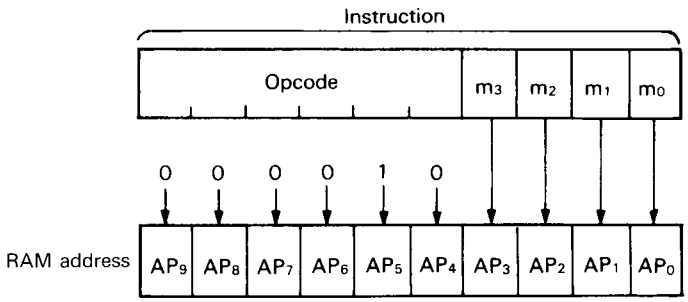
The P instruction has no effect on the program counter.



Register Indirect Addressing



Direct Addressing



Memory Register Addressing

Figure 17 RAM Addressing Modes

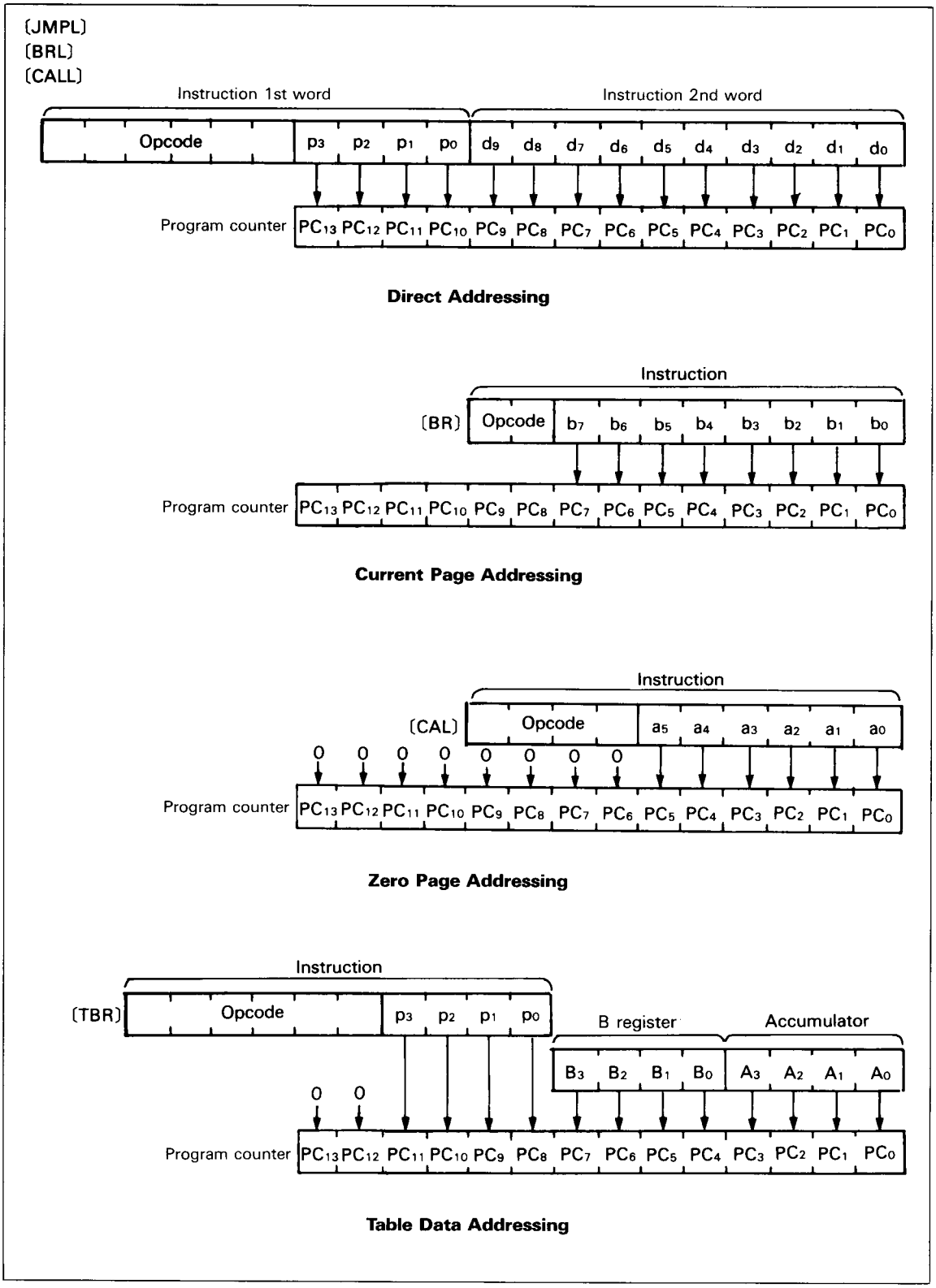


Figure 18 ROM Addressing Modes

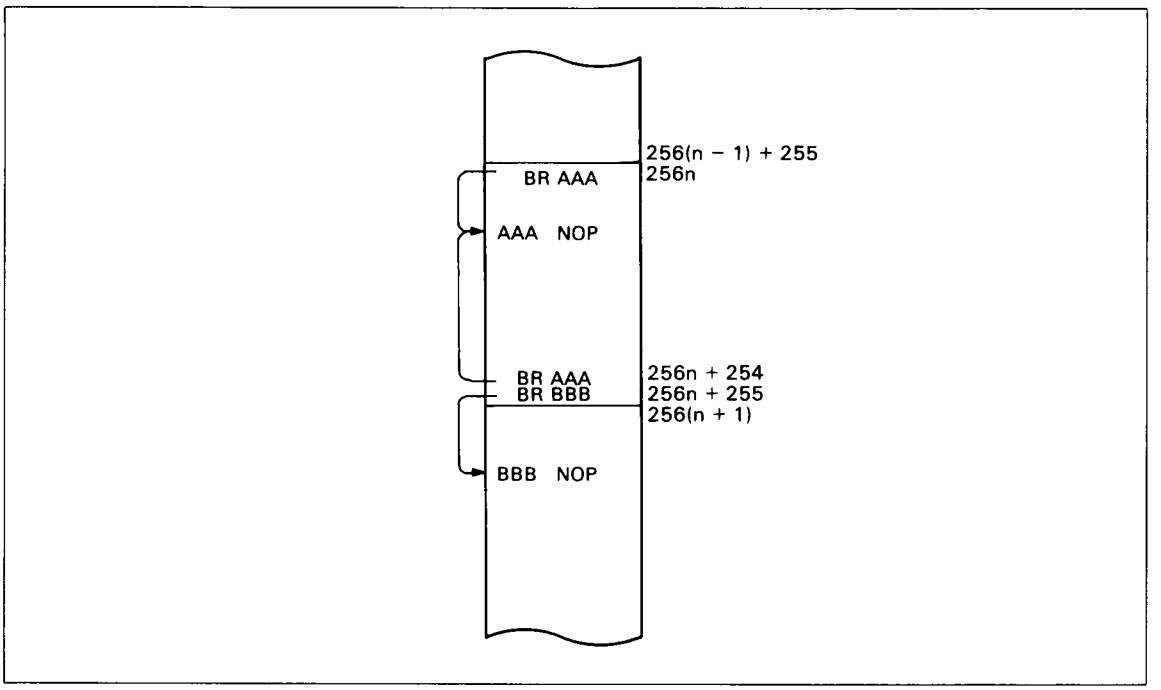


Figure 19 BR Instruction Branch Destination on a Page Boundary

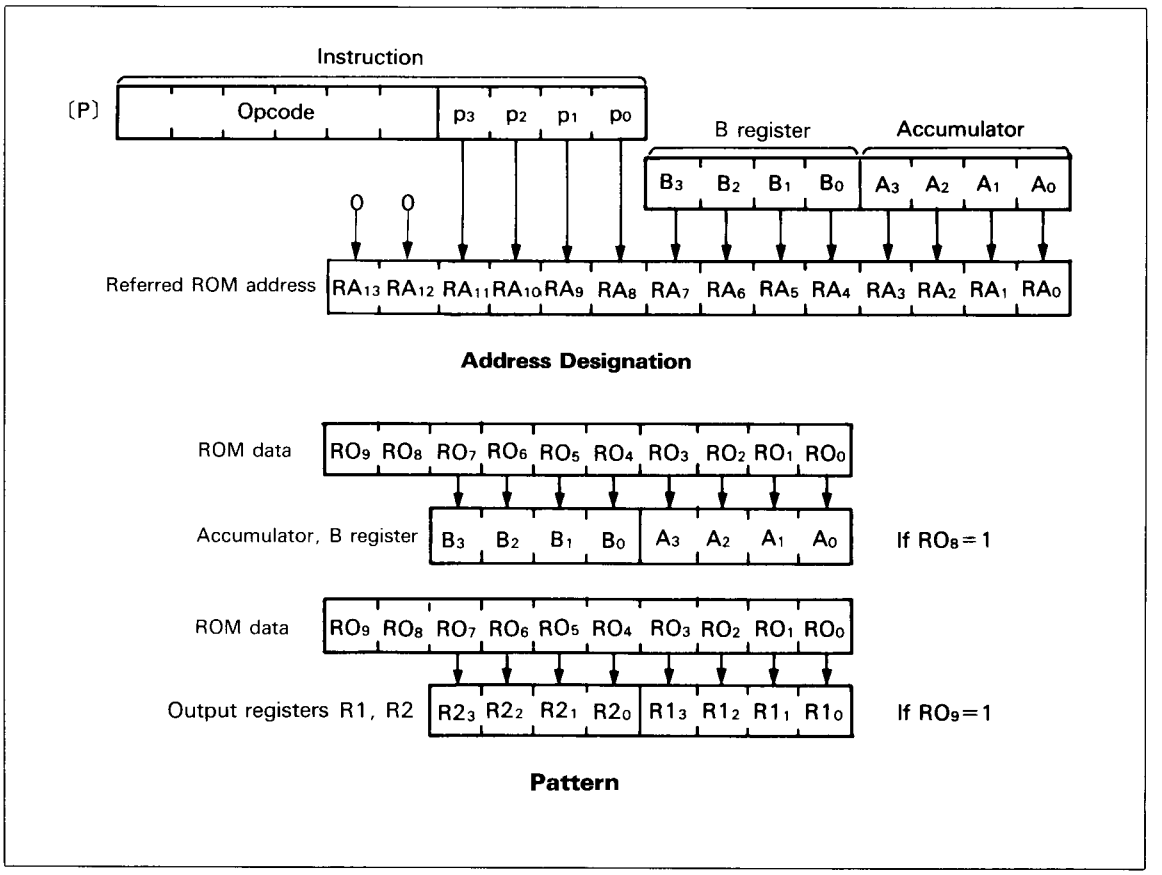


Figure 20 P Instruction

Precautions on using EPROM On-Package Type Microcomputer

Since the HD40P4919 is specially structured with pin sockets on the surface of its package, the following should be noted when using it.

1. Do not apply an electrostatic voltage or surge voltage more than the maximum ratings to the pin sockets. This may destroy the LSI permanently.
2. When installing this LSI in system products in the same way as the mask ROM 4-bit single chip microcomputer, observe the following in order to maintain good ohmic contact between EPROM pins and pin sockets.
   a. When soldering the LSI on a printed circuit board, keep pin conditions under 250°C within 10 seconds. If these conditions are exceeded, the solder fixing of the pin sockets may melt and the pins may fall out.
   b. Detergent and coatings must be kept out from the pin sockets during flux removal or board coating. Flux or coatings may decrease pin contact within the pin sockets.
   c. Avoid permanent use of this LSI in places with excessive vibration.
   d. Since repeated insertion/removal of EPROMs may decrease the contact within the pin sockets, it is recommended to use new ones for your system products.

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Supply voltage	V_{CC}	−0.3 to +7.0	V	
Pin voltage	V_T	−0.3 to V_{CC} + 0.3	V	3
		−0.3 to +15	V	4
Total permissible input current	ΣI_o	200	mA	5
Maximum input current	I_o	15	mA	7, 8
		35	mA	7, 10
Maximum output current	$-I_o$	4	mA	8, 9
Total permissible output current	$-\Sigma I_o$	50	mA	6
Operating temperature	T_{opr}	−20 to +75	°C	
Storage temperature	T_{stg}	−55 to +125	°C	

Notes: 1. Permanent damage may occur if these absolute maximum ratings are exceeded. Normal operation should be under the conditions of the electrical characteristics tables. If these conditions are exceeded, the LSI may malfunction or its reliability may be affected.
2. All voltages are with respect to GND.
3. Standard pins.
4. High-voltage pins.
5. Total permissible input current is the total sum of input currents which flow in from all I/O pins to GND simultaneously.
6. Total permissible output current is the total sum of the output currents which flow out from V_{CC} to all I/O pins simultaneously.
7. Maximum input current is the maximum amount of input current from each I/O pin to GND.
8. D_0-D_{14}, R3-R4, and R0
9. Maximum output current is the maximum amount of output current from V_{CC} to each I/O pin.
10. R1-R2.

Electrical Characteristics

HD404918 Electrical Characteristics

DC Characteristics (V_{CC} = 4 to 6 V, GND = 0 V, T_a = −20° to +75°C, unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	RESET, $\overline{INT_0}$, $\overline{INT_1}$	0.8V_{CC}		V_{CC} + 0.3	V		
		OSC_1	V_{CC} − 0.5		V_{CC} + 0.3	V		
Input low voltage	V_{IL}	RESET, $\overline{INT_0}$, $\overline{INT_1}$	−0.3		0.2V_{CC}	V		
		OSC_1	−0.3		0.5	V		
Input/output leakage current	$\lvert I_{IL} \rvert$	RESET, $\overline{INT_0}$, $\overline{INT_1}$, OSC_1			1	μA	V_{in} = 0 V to V_{CC}	1
Current dissipation in active mode	I_{CC}	V_{CC}			2.5	mA	V_{CC} = 5 V; f_{OSC} = 4 MHz, divide-by-8	2, 5
Current dissipation in standby mode	I_{SBY}	V_{CC}			1.0	mA	V_{CC} = 5 V; f_{OSC} = 4 MHz, divide-by-8	3, 5
Current dissipation in stop mode	I_{STOP}	V_{CC}			10	μA	$V_{in(\overline{TEST})}$ = V_{CC} − 0.3 V to V_{CC}, $V_{in(RESET)}$ = 0 V to 0.3 V	4
Stop mode retaining voltage	V_{STOP}	V_{CC}	2			V		

Notes: 1. Excluding pull-up MOS current and output buffer current.
2. The MCU is in the reset state. Input/output current does not flow.
   - MCU in reset state, operation mode
   - RESET, $\overline{TEST}$: V_{CC}
   - D_0-D_{14}, R0-R4: V_{CC}
3. The timer/counter operates with the fastest clock. Input/output current does not flow.
   - MCU in standby mode
   - Input/output in reset state
   - RESET: GND
   - $\overline{TEST}$: V_{CC}
   - D_0-D_{14}, R0-R4: V_{CC}
4. Excluding pull-up MOS current.
5. When f_{OSC} = x MHz, the current dissipation can be estimated as follows:
   Maximum value (at x MHz) = (x/4) × (max. value at 4 MHz)

Input/Output Characteristics for Standard Pins (V_{CC} = 4 to 6 V, GND = 0 V, T_a = −20° to +75°C, unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	R1-R2	0.7V_{CC}		V_{CC} + 0.3	V		3
		D_0-D_{14}, R3-R4						4
Input low voltage	V_{IL}	R1-R2	−0.3		0.3V_{CC}	V		3
		D_0-D_{14}, R3-R4						4
Output high voltage	V_{OH}	D_0-D_{14}, R3-R4, R0	V_{CC} − 1.0			V	$-I_{OH}$ = 1.0 mA	1
		D_0-D_{14}, R3-R4, R0	V_{CC} − 0.5			V	$-I_{OH}$ = 0.5 mA	1
Output low voltage	V_{OL}	D_0-D_{14}, R3-R4, R0			0.4	V	I_{OL} = 1.6 mA	
		R1-R2			1.0	V	V_{CC} = 5 V, I_{OL} = 25 mA	3
Input/output leakage current	$\lvert I_{IL} \rvert$	D_0-D_{14}, R3-R4, R0			1	μA	V_{in} = 0 V to V_{CC}	2
		R1-R2			20			
Pull-up MOS current	$-I_p$	D_0-D_{14}, R3-R4, R0	30	90	170	μA	V_{CC} = 5 V, V_{in} = 0 V	4

Notes: 1. Applied to I/O pins selected as CMOS output by mask option.
2. Pull-up MOS current and output buffer current are excluded.
3. Applied to I/O pins selected as without pull-up MOS by mask option.
4. Selected as with pull-up MOS by mask option.

Input/Output Characteristics for High Voltage Pins (V_{CC} = 4 to 6 V, GND = 0 V, T_a = −20° to +75°C, unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Input high voltage	V_{IH}	D_0-D_{14}, R3-R4	0.7V_{CC}		12	V		1
Input low voltage	V_{IL}	D_0-D_{14}, R3-R4	−0.3		0.3V_{CC}	V		1
Output high voltage	V_{OH}	D_0-D_{14}, R3-R4, R0	11.5			V	500 kΩ at 12 V	1
Output low voltage	V_{OL}	D_0-D_{14}, R3-R4, R0			0.4	V	I_{OL} = 1.6 mA	1
Input/output leakage current	$\lvert I_{IL} \rvert$	D_0-D_{14}, R3-R4, R0			1	μA	V_{in} = 0 V to V_{CC}	1

Note: 1. Applied to I/O pins selected as without pull-up MOS by mask option.

AC Characteristics (V_{CC} = 4 to 6 V, GND = 0 V, T_a = −20° to +75°C, unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Oscillation frequency	f_{OSC}	OSC_1, OSC_2	0.4	4	4.5	MHz	Divide-by-8	
Instruction cycle time	t_{cyc}		1.78	2	20	μs		
Oscillator stabilization time	t_{RC}	OSC_1, OSC_2			20	ms		1
External clock frequency	f_{cp}	OSC_1	0.4		4.5	MHz		2
External clock high and low widths	t_{CPH}, t_{CPL}	OSC_1	92			ns	Divide-by-8	2
External clock rise time	t_{CPr}	OSC_1			20	ns		2
External clock fall time	t_{CPf}	OSC_1			20	ns		2
Instruction cycle time	t_{cyc}		1.78		20	μs		2
$\overline{INT_0}$ high width	t_{I0H}	$\overline{INT_0}$	2			t_{cyc}		3
$\overline{INT_0}$ low width	t_{I0L}	$\overline{INT_0}$	2			t_{cyc}		3
$\overline{INT_1}$ high width	t_{I1H}	$\overline{INT_1}$	2			t_{cyc}		3
$\overline{INT_1}$ low width	t_{I1L}	$\overline{INT_1}$	2			t_{cyc}		3
RESET high width	t_{RSTH}	RESET	2			t_{cyc}		4
Input capacitance	C_{in}	All pins			15	pF	f = 1 MHz, V_{in} = 0 V	
RESET fall time	t_{RSTf}				20	ms		4

Notes: 1. The oscillator stabilization time is the period from when V_{CC} reaches its minimum allowable voltage 4 V at power-on until when the oscillator stabilizes, or after RESET goes high. At power-on or recovering from stop mode, RESET must be kept high for more than t_{RC}. Since t_{RC} depends on the crystal or ceramic filter's circuit constant and stray capacitance, consult with the ceramic filter manufacturer when designing the circuit. (See figure 21.)
2. See figure 22.
3. See figure 23.
4. See figure 24.

HD404919 Electrical Characteristics

DC Characteristics (V_{CC} = 4 to 6 V, GND = 0 V, T_a = −20° to +75°C, unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	RESET	0.85V_{CC}		V_{CC} + 0.3	V		
		$\overline{INT_0}$, $\overline{INT_1}$	0.8V_{CC}		V_{CC} + 0.3	V		
		OSC_1	V_{CC} − 0.5		V_{CC} + 0.3	V		
Input low voltage	V_{IL}	RESET	−0.3		0.15V_{CC}	V		
		$\overline{INT_0}$, $\overline{INT_1}$	−0.3		0.2V_{CC}	V		
		OSC_1	−0.3		0.5	V		
Input/output leakage current	$\lvert I_{IL} \rvert$	RESET, $\overline{INT_0}$, $\overline{INT_1}$, OSC_1			1	μA	V_{in} = 0 V to V_{CC}	1
Current dissipation in active mode	I_{CC}	V_{CC}			6.5	mA	V_{CC} = 5 V; f_{OSC} = 8 MHz, divide-by-8	2, 5
Current dissipation in standby mode	I_{SBY}	V_{CC}			1.8	mA	V_{CC} = 5 V; f_{OSC} = 8 MHz, divide-by-8	3, 5
Current dissipation in stop mode	I_{STOP}	V_{CC}			10	μA	$V_{in(\overline{TEST})}$ = V_{CC} − 0.3 V to V_{CC}, $V_{in(RESET)}$ = 0 V to 0.3 V	4
Stop mode retaining voltage	V_{STOP}	V_{CC}	2			V		

Notes: 1. Excluding pull-up MOS current and output buffer current.
2. The MCU is in the reset state. Input/output current does not flow.
   - MCU in reset state, operation mode
   - RESET, $\overline{TEST}$: V_{CC}
   - D_0-D_{14}, R0-R4: V_{CC}
3. The timer/counter operates with the fastest clock. Input/output current does not flow.
   - MCU in standby mode
   - Input/output in reset state
   - RESET: GND
   - $\overline{TEST}$: V_{CC}
   - D_0-D_{14}, R0-R4: V_{CC}
4. Excluding pull-up MOS current.
5. When f_{OSC} = x MHz, the current dissipation can be estimated as follows:
   Max. value (at x MHz) = (x/8) × (max. value at 8 MHz)

Input/Output Characteristics for Standard Pins (V_{CC} = 4 to 6 V, GND = 0 V, T_a = −20° to +75°C, unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	R1-R2	0.7V_{CC}		V_{CC} + 0.3	V		3
		D_0-D_{14}, R3-R4						4
Input low voltage	V_{IL}	R1-R2	−0.3		0.3V_{CC}	V		3
		D_0-D_{14}, R3-R4						4
Output high voltage	V_{OH}	D_0-D_{14}, R3-R4, R0	V_{CC} − 1.0			V	$-I_{OH}$ = 1.0 mA	1
		D_0-D_{14}, R3-R4, R0	V_{CC} − 0.5			V	$-I_{OH}$ = 0.5 mA	1
Output low voltage	V_{OL}	D_0-D_{14}, R3-R4, R0			0.4	V	I_{OL} = 1.6 mA	
		R1-R2			1.0	V	V_{CC} = 5 V, I_{OL} = 25 mA	3
Input/output leakage current	$\lvert I_{IL} \rvert$	D_0-D_{14}, R3-R4, R0			1	μA	V_{in} = 0 V to V_{CC}	2
		R1-R2			20			
Pull-up MOS current	$-I_p$	D_0-D_{14}, R3-R4, R0	30	60	150	μA	V_{CC} = 5 V, V_{in} = 0 V	4

Notes: 1. Applied to I/O pins selected as CMOS output by mask option.
2. Pull-up MOS current and output buffer current are excluded.
3. Applied to I/O pins selected as without pull-up MOS by mask option.
4. Selected as with pull-up MOS by mask option.

Input/Output Characteristics for High Voltage Pins (V_{CC} = 4 to 6 V, GND = 0 V, T_a = −20° to +75°C, unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	D_0-D_{14}, R3-R4	0.7V_{CC}		12	V		1
Input low voltage	V_{IL}	D_0-D_{14}, R3-R4	−0.3		0.3V_{CC}	V		1
Output high voltage	V_{OH}	D_0-D_{14}, R3-R4, R0	11.5			V	500 kΩ at 12 V	1
Output low voltage	V_{OL}	D_0-D_{14}, R3-R4, R0			0.4	V	I_{OL} = 1.6 mA	1
Input/output leakage current	$\lvert I_{IL} \rvert$	D_0-D_{14}, R3-R4, R0			1	μA	V_{in} = 0 V to V_{CC}	1

Note: 1. Applied to I/O pins selected as without pull-up MOS by mask option.

AC Characteristics (V_{CC} = 4 to 6 V, GND = 0 V, T_a = −20° to +75°C, unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Oscillation frequency	f_{OSC}	OSC_1, OSC_2	0.4	8	9	MHz	Divide-by-8	
Instruction cycle time	t_{cyc}		0.89	1	20	μs		
Oscillator stabilization time	t_{RC}	OSC_1, OSC_2			20	ms		1
External clock frequency	f_{cp}	OSC_1	0.4	8	9	MHz		2
External clock high and low widths	t_{CPH}, t_{CPL}	OSC_1	41			ns	Divide-by-8	2
External clock Rise time	t_{CPr}	OSC_1			15	ns		2
External clock Fall time	t_{CPf}	OSC_1			15	ns		2
Instruction cycle time	t_{cyc}		0.89	1	20	μs		2
$\overline{INT_0}$ high width	t_{I0H}	$\overline{INT_0}$	2			t_{cyc}		3
$\overline{INT_0}$ low width	t_{I0L}	$\overline{INT_0}$	2			t_{cyc}		3
$\overline{INT_1}$ high width	t_{I1H}	$\overline{INT_1}$	2			t_{cyc}		3
$\overline{INT_1}$ low wdth	t_{I1L}	$\overline{INT_1}$	2			t_{cyc}		3
RESET high width	t_{RSTH}	RESET	2			t_{cyc}		4
Input capacitance	C_{in}	All pins			15	pF	f = 1 MHz, V_{in} = 0 V	
RESET fall time	t_{RSTf}				20	ms		4

Notes: 1. The oscillator stabilization time is the period from when V_{CC} reaches its minimum allowable voltage 4 V at power-on until when the oscillator stabilizes, or after RESET goes high. At power-on or recovering from stop mode, RESET must be kept high for more than t_{RC}. Since t_{RC} depends on the crystal or ceramic filter's circuit constant and stray capacitance, consult with the ceramic filter manufacturer when designing the circuit. (See figure 21.)
2. See figure 22.
3. See figure 23.
4. See figure 24.

HD40P4919 Electrical Characteristics

DC Characteristics (V_{CC} = 4.5 to 5.5 V, GND = 0 V, T_a = −20° to +75°C, unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	RESET	0.85V_{CC}		V_{CC} + 0.3	V		
		$\overline{INT_0}$, $\overline{INT_1}$	0.8V_{CC}		V_{CC} + 0.3	V		
		OSC_1	V_{CC} − 0.5		V_{CC} + 0.3	V		
Input low Voltage	V_{IL}	RESET	−0.3		0.15V_{CC}	V		
		$\overline{INT_0}$, $\overline{INT_1}$	−0.3		0.2V_{CC}	V		
		OSC_1	−0.3		0.5	V		
Input/output leakage current	$\lvert I_{IL} \rvert$	RESET, $\overline{INT_0}$, $\overline{INT_1}$, OSC_1			1	μA	V_{in} = 0 V to V_{CC}	1
Current dissipation in active mode	I_{CC}	V_{CC}			5	mA	V_{CC} = 5 V; f_{OSC} = 8 MHz, divide-by-8	2, 4
Current dissipation in standby mode	I_{SBY}	V_{CC}			2.6	mA	V_{CC} = 5 V; f_{OSC} = 8 MHz, divide-by-8	3, 4
Current dissipation in stop mode	I_{STOP}	V_{CC}			10	μA	$V_{in(\overline{TEST})}$ = V_{CC} − 0.3 V to V_{CC}, $V_{in(RESET)}$ = 0 V to 0.3 V	
Stop mode retaining voltage	V_{STOP}	V_{CC}	2			V		

Notes: 1. Output buffer current are excluded.
2. The MCU is in the reset state. Input/output current does not flow.
   - MCU in reset state, operation mode
   - RESET, $\overline{TEST}$: V_{CC}
   - D_0-D_{14}, R0-R4: V_{CC}
3. The timer/counter operates with the fastest clock. Input/output current does not flow.
   - MCU in standby mode
   - Input/output in reset state
   - RESET: GND
   - $\overline{TEST}$: V_{CC}
   - D_0-D_{14}, R0-R4: V_{CC}
4. When f_{OSC} = x MHz, the current dissipation can be estimated as follows:
   Max. value (at x MHz) = (x/8) × (max. value at 8 MHz)

Input/Output Characteristics for Standard Pins (V_{CC} = 4.5 to 5.5 V, GND = 0 V, T_a = −20° to +75°C, unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition
Input high voltage	V_{IH}	R1-R2	0.7V_{CC}		V_{CC} + 0.3	V	
Input low voltage	V_{IL}	R1-R2	−0.3		0.3V_{CC}	V	
Output low voltage	V_{OL}	R1-R2			1.2	V	V_{CC} = 5 V, I_{OL} = 25 mA
Input/output leakage current Note	$\lvert I_{IL} \rvert$	R1-R2			20	μA	V_{in} = 0 V to V_{CC}

Note: Output buffer current are excluded.

Input/Output Characteristics for High Voltage Pins (V_{CC} = 4.5 to 5.5 V, GND = 0 V, T_a = −20° to +75°C, unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition
Input high voltage	V_{IH}	D_0-D_{14}, R3-R4	0.7V_{CC}		12	V	
Input low voltage	V_{IL}	D_0-D_{14}, R3-R4	−0.3		0.3V_{CC}	V	
Output high voltage	V_{OH}	D_0-D_{14}, R3-R4, R0	11.5			V	500 kΩ at 12 V
Output low voltage	V_{OL}	D_0-D_{14}, R3-R4, R0			0.4	V	I_{OL} = 1.6 mA
Input/output leakage current Note	$\lvert I_{IL} \rvert$	D_0-D_{14}, R3-R4, R0			1	μA	V_{in} = 0 V to V_{CC}

Note: Output buffer current are excluded.

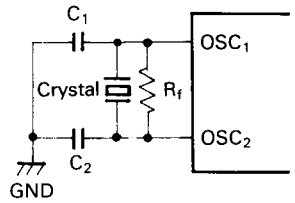
AC Characteristics (V_{CC} = 4.5 to 5.5 V, GND = 0 V, T_a = −20° to +75°C, unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Oscillation frequency	f_{OSC}	OSC_1, OSC_2	0.4	8	9	MHz	Divide-by-8	
Instruction cycle time	t_{cyc}		0.89	1	20	μs		
Oscillator stabilization time	t_{RC}	OSC_1, OSC_2			20	ms		1
External clock frequency	f_{cp}	OSC_1	0.4	8	9	MHz		2
External clock high and low widths	t_{CPH}, t_{CPL}	OSC_1	41			ns	Divide-by-8	2
External clock rise time	t_{CPr}	OSC_1			15	ns		2
External clock fall time	t_{CPf}	OSC_1			15	ns		2
Instruction cycle time	t_{cyc}		0.89	1	20	μs		2
$\overline{INT_0}$ high width	t_{I0H}	$\overline{INT_0}$	2			t_{cyc}		3
$\overline{INT_0}$ low width	t_{I0L}	$\overline{INT_0}$	2			t_{cyc}		3
$\overline{INT_1}$ high width	t_{I1H}	$\overline{INT_1}$	2			t_{cyc}		3
$\overline{INT_1}$ low width	t_{I1L}	$\overline{INT_1}$	2			t_{cyc}		3
RESET high width	t_{RSTH}	RESET	2			t_{cyc}		4
Input capacitance	C_{in}	All pins			15	pF	f = 1 MHz, V_{in} = 0 V	
RESET fall time	t_{RSTf}				20	ms		4

Notes: 1. The oscillator stabilization time is the period from when V_{CC} reaches its minimum allowable voltage 4.5 V at power-on until when the oscillator stabilizes, or after RESET goes high. At power-on or recovering from stop mode, RESET must be kept high for more than t_{RC}. Since t_{RC} depends on the crystal or ceramic filter's circuit constant and stray capacitance, consult with the ceramic filter manufacturer when designing the circuit. (See figure 21.)
2. See figure 22.
3. See figure 23.
4. See figure 24.

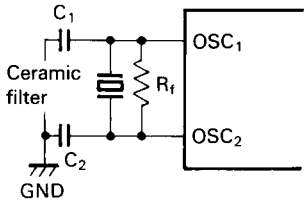
HD404918

Crystal oscillator



Crystal : 4.194304 MHz NC-18C (Nihon Denpa Kogyo)
R_f : 1 MΩ ± 20 %
C_1 : 22 pF ± 20%
C_2 : 22 pF ± 20%

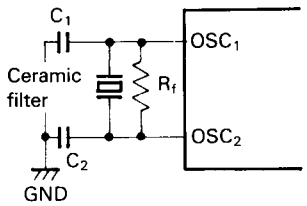
Ceramic filter oscillator



Ceramic filter : CSA 4.00 MG (Murata)
R_f : 1 MΩ ± 20%
C_1 : 30 pF ± 20%
C_2 : 30 pF ± 20%

HD404919, HD40P4919

Ceramic filter oscillator



Ceramic filter : CSA8.00MT (Murata)
R_f : 1 MΩ ± 20 %
C_1 : 30 pF ± 20%
C_2 : 30 pF ± 20%

Figure 21 Oscillator Circuits

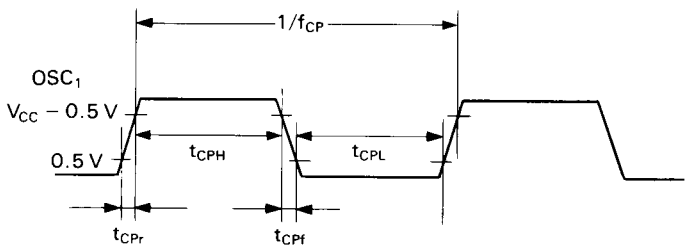


Figure 22 Oscillator Timing

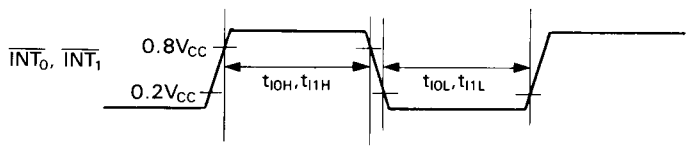
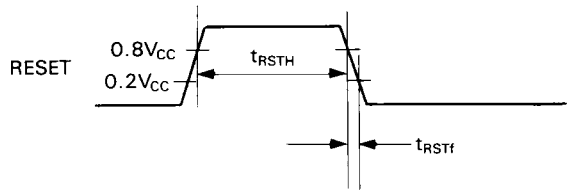


Figure 23 Interrupt Timing

HD404918



HD404919, HD40P4919

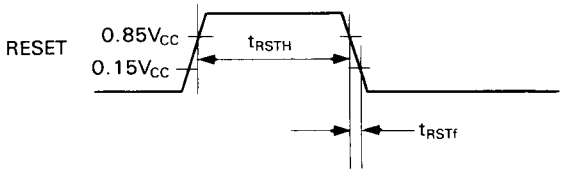


Figure 24 Reset Timing

HD404918/HD404919 Mask Option List

Date of order	
Customer	
Department	
Name	
ROM code name	
LSI type number (Hitachi's entry)	

I/O Option

Please check off the applicable items for the I/O option selection.
A: Without pull-up MOS (NMOS open drain) B: With pull-up MOS
C: CMOS output (not be used as input)

Note: I/O options masked by ▨ are not available.

Pin		Input/Output	I/O Option A	B	C
D_0		Input/Output			
D_1		Input/Output			
D_2		Input/Output			
D_3		Input/Output			
D_4		Input/Output			
D_5		Input/Output			
D_6	*2	Input/Output			
D_7		Input/Output			
D_8		Input/Output			
D_9		Input/Output			
D_{10}		Input/Output			
D_{11}		Input/Output			
D_{12}		Input/Output			
D_{13}		Input/Output			
D_{14}		Input/Output			

Pin			Input/Output	I/O Option A	B	C
R0	$R0_0$	*2	Output			
	$R0_1$		Output			
	$R0_2$		Output			
	$R0_3$		Output			
R1	$R1_0$	*1	Input/Output		▨	▨
	$R1_1$		Input/Output		▨	▨
	$R1_2$		Input/Output		▨	▨
	$R1_3$		Input/Output		▨	▨
R2	$R2_0$		Input/Output		▨	▨
	$R2_1$		Input/Output		▨	▨
	$R2_2$		Input/Output		▨	▨
	$R2_3$		Input/Output		▨	▨
R3	$R3_0$		Input/Output			
	$R3_1$		Input/Output			
	$R3_2$		Input/Output			
	$R3_3$		Input/Output			
R4	$R4_0$	*2	Input/Output			
	$R4_1$		Input/Output			
	$R4_2$		Input/Output			
	$R4_3$		Input/Output			

Notes *1. High current pins.
*2. High voltage pins only when I/O option A is selected.

ROM Code Media

Please check off applicable items by ■, X, or √.

ROM Code Media
☐ EPROM: For emulator
☐ EPROM: For on-package microcomputer

Application Check List

Oscillator (CPG Option)

Please check off applicable items by ■, X, or √.

☐ Crystal or ceramic filter	(HD404918)
☐ Ceramic filter	(HD404919)